NOAO
MONSOON
Image Acquisition System

Concept Design Review

Barry Michael Starr
Nick Buchholz

12/8/2006
MONSOON Presentation Overview

- Motivation
- Fundamental System Design Concepts
- System Hardware Architecture
- System Implementations
- System Software Architecture
- Project Management Issues
- Discussion
MONSOON Motivation

Barry Michael Starr
MONSOON Motivation

- Existing NOAO Systems Based on Obsolete Component
  - InMOS Transputer Discontinued
- Existing NOAO Systems Unable to Adequately Support Next Generation Projects Primarily Due to the Following:
  - High Channel Counts
  - High Aggregate Data Rates
Why MONSOON?
Why Not NDAS…

- A Rose by Any Other Name…
  - No, No, Please Not Another Tortured Acronym…
- CCD Analogy with Photons as Raindrops…
  - Somebody Bring Me a Bucket…

Figure 1.7(a) Bucket analogy used to describe CCD operation.
Defined MONSOON Applications

- **ORION 2K X 2K InSb & HgCdTe Development**
  - (64 Channels @ 1.5uS/pixel/output)

- **NEWFIRM 4K x 4K IR Imager**
  - (128 to 256 Channels @ 1.5 to 3uS/pixel/output)

- **WIYN QUOTA 8k x 8k OT Imager**
  - (32 Channels @ 1 uS/Pixel/Output)

- **LBNL MiniMOSAIC**
  - (8 Channels @ 5us/Pixel/Output)

* Detector-Limited Performance Specifications
Potential MONSOON Applications

• One Degree Imager (ODI) for WYIN
• LSST
• Gemini GSAO IR Imager
• TSIP / SWIFT / GSMT Instruments
• NGOS
• 8k x 8k IR Camera (Columbia University)
• NGST Detector Lab Support
• Upgrade Existing Systems (MOSAIC/MiniMOSAIC)
# RIO (SBRC) ORION 2k x 2k (InSb/HgCdTe)

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout Channels</td>
<td>64 Channels</td>
</tr>
<tr>
<td>ReadNoise</td>
<td>20e-</td>
</tr>
<tr>
<td>Gain (uV/e-)</td>
<td>2</td>
</tr>
<tr>
<td>Pixel Rate/Output</td>
<td>1.5 μS per output</td>
</tr>
<tr>
<td>Full Well (1% Linearity)</td>
<td>300,000e-</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>&gt; 16-bit</td>
</tr>
<tr>
<td>Image Size</td>
<td>2k x 2k = 4M pixels</td>
</tr>
<tr>
<td>Readout Time</td>
<td>100mS (ORION projected limit, 10Hz Frame Rate)</td>
</tr>
<tr>
<td>Data Rate</td>
<td>4M pix/100mS = 40M pix/S (10 Hz Rate)</td>
</tr>
<tr>
<td>Systran SL100 supports</td>
<td>50Mpix/S (10 Hz Rate)</td>
</tr>
<tr>
<td>Clock &amp; Bias Requirements</td>
<td>8 Clocks (-2V to –7V Range)</td>
</tr>
<tr>
<td></td>
<td>18 Biases/Clocked Biases (0 to –8V Range)</td>
</tr>
</tbody>
</table>

12/8/2006
NEWFIRM FPA Candidates

- Rockwell HAWAII-2 HgCdTe 4k x 4k Implementation
  - Non-Buttable LCC Package Exists
  - 4-side Buttable Package Under Development
  - Pre Assembled 4k x 4k Module Under Discussion
- Rockwell “Digital FPA” HgCdTe 4k x 4k Implementation
  - Under Discussion, Interface and Packaging TDB

- RIO (SBRC) Orion (InSb/HgCdTe) 4k x 4k Implementation
  - 2-Side Buttable 2k x 2k Package Exists
  - Pre-Assembled 4k x 4k Module Under Discussion
### NEWFIRM Implementation

**Rockwell HAWAII-2 (1-2.5um)**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout Channels:</td>
<td>$4 \times 32 (36) = 128 (144)$ Channels</td>
</tr>
<tr>
<td>ReadNoise:</td>
<td>$&gt;10e^{-}$ (Typically $13-20e^{-}$)</td>
</tr>
<tr>
<td>Gain (uV/e-):</td>
<td>3-6</td>
</tr>
<tr>
<td>Pixel Rate/Output:</td>
<td>4 uS per output</td>
</tr>
<tr>
<td>Full Well</td>
<td>$100,000e^{-}$</td>
</tr>
<tr>
<td>Dynamic Range:</td>
<td>16-bit</td>
</tr>
<tr>
<td>Image Size</td>
<td>$4 \times 2048 \times 2048 = 16M$ pixels</td>
</tr>
<tr>
<td>Readout Time</td>
<td>$\sim 500$ mS ($\sim 2$Hz Frame Rate)</td>
</tr>
<tr>
<td>Data Rate</td>
<td>$16M$ pix/500mS = $32Mpix/S$</td>
</tr>
<tr>
<td></td>
<td>$&lt; 50M$ pix/S (SL100 rate)</td>
</tr>
<tr>
<td>Clock &amp; Bias Requirements</td>
<td>$13 \times 4 = 52$ Clocks (CMOS Inputs, 0-5V Range)</td>
</tr>
<tr>
<td></td>
<td>$5 \times 4 = 20$ Biases (0 to 5V Range)</td>
</tr>
</tbody>
</table>
## NEWFIRM Implementation

### RIO ORION (1-2.5μm)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Readout Channels:</strong></td>
<td>$4 \times 64 = 256$ Channels</td>
</tr>
<tr>
<td><strong>ReadNoise:</strong></td>
<td>$20e^{-}$</td>
</tr>
<tr>
<td><strong>Gain (μV/e-):</strong></td>
<td>2</td>
</tr>
<tr>
<td><strong>Pixel Rate/Output</strong></td>
<td>1.5 μS per output</td>
</tr>
<tr>
<td><strong>Full Well (1% Linearity)</strong></td>
<td>$300,000e^{-}$</td>
</tr>
<tr>
<td><strong>Dynamic Range:</strong></td>
<td>$&gt;16$-bit</td>
</tr>
<tr>
<td><strong>Image Size</strong></td>
<td>$4 \times 2k \times 2k = 16M$ pixels</td>
</tr>
<tr>
<td><strong>Readout Time</strong></td>
<td>100mS (ORION projected limit, 10Hz Frame Rate)</td>
</tr>
<tr>
<td></td>
<td>2.5S (based on 2.5μm background per R.Probst)</td>
</tr>
<tr>
<td><strong>Data Rate</strong></td>
<td>$16M$ pix/100mS = 160M pix/S (10 Hz Rate)</td>
</tr>
<tr>
<td></td>
<td>Systran SL240 supports 120Mpix/S (7 Hz Rate)</td>
</tr>
<tr>
<td><strong>Clock &amp; Bias Requirements</strong></td>
<td>$8 \times 4 = 32$ Clocks (-2V to –7V Range)</td>
</tr>
<tr>
<td></td>
<td>$18 \times 4 = 72$ Biases/Clocked Biases (0 to –8V Range)</td>
</tr>
</tbody>
</table>

*12/8/2006*
QUOTA-Quad Orthogonal Transfer Array

- A new paradigm in large imagers

OTCCD pixel structure

Basic OTCCD cell

OTA: 8x8 array of OTCCDs
Each CCD cell of a 4Kx4K OTA
- Independent 512x512 CCD
  - Individual or collective addressing
  - 1 arcmin field of view
- Dead cells excised, yield >50%
  - Bad columns confined to cells
- Cells with bright stars for guiding
- 8 output channels per OTA
  - Fast readout (8 amps, 2 sec)
- Disadvantage -- 0.1 mm gaps, but gaps and dead cells are dithered out anyway

12/8/2006
QUOTA (8k x 8k) for WIYN
Package & Demonstration Camera

- 4-side buttable package w/ multilayer ceramic substrate
- Flexprint to hermetic or through wall
- Cryocooled bars
- Four OTAs = QUOTA
  (8K x 8K = 15 x 15 arcmin)

12/8/2006
WIYN One Degree Imager

- Instrumentation goal for WIYN
- 64 OTAs = ODI
  - (32K x 32K = 1 x 1 deg)
- QUOTA does the R&D,
- different funding for
  - large cryostat,
  - additional devices,
  - filters, shutter, etc.
- Deployment in 2005
Implementing the Decadal Survey
Large Synoptic Survey Telescope (LSST)

- 6-8m equivalent aperture
- 3 degree Field of View (FOV)
- Curved Focal Plane
- 1400 1k x 1k CCDs (or ???)
- “National Virtual Observatory” (NVO)
Visible MOSAIC Development Path

- **QUOTA**: 8K
- **ODI**: 32K (~$4M)
- **LSST**: 37K
Traditional Mosaic Imagers

- Too expensive
- Too slow
- Poor red response

Figure of merit:

\[ M = \frac{A \Omega \varepsilon}{d\theta^2} \]

Collecting area A may be fixed, but we can improve all three other factors.
MONSOON
Fundamental Design Concepts
MONSOON Image Acquisition System

- Scalable Multi-Channel High-Speed Image Acquisition System
- Scalable at All Levels Based on Cost/Performance System Trade-offs
- Specifically Designed to Address the Needs of Next-Generation IR & CCD Mosaic Systems
  - ORION (2k x 2k) InSb & HgCdTe Development
  - NEWFIRM (4k x 4k)
  - WYIN QUOTA (8k x 8k) => ODI (32k x 32k)
  - LSST (38k x 38k)
- Increased Performance Over Existing Solutions
  - With Reduced Cost
  - With Reduced Size
  - With Reduced Power Consumption
Systems Design Approach to MONSOON

- Investigate Requirements,
  - Interview All Stakeholders, Astros & Tech Staff (NOAO/KPNO/CTIO)
- Analyze and Document Existing Systems
- Define Requirements
- Evaluate Existing Solutions/Technologies
- Develop Plan
- Implement Plan
- Deliver System
- Evaluate Project Performance
Existing Systems Evaluated

- ESO FIERA (CCDs)
- ESO IRACE (IR Detectors)
- CFHT MEGACAM (CCD)
- SAO MEGACAM (CCD)
- IRTF SPEX/ RedStar 2 Controller (IR Detectors)
- Subaru MESSIA/MFRONT Electronics (CCD)
- MFRONT Electronics (CCD used on QUEST)
- University of Florida FLAMINGOS (IR Detectors)
- Italian National Observatory Controller (CCD)
- SDSU II (CCD and IR Detectors)
- PIXCELENT (CCD)
- National Instruments PXI Based Instrumentation
System Evaluation Criteria

1) Performance
   Scalability / Range of Devices Supported

2) Total System Cost (Manpower and Materials)
   Purchase Price / Integration Costs / Maintenance Costs

3) Availability

4) Vendor Support / User Base

5) Documentation

6) Calibration

7) Expected Lifetime
   Use of Standard or Obsolete Technologies

8) Power Consumption

9) Form Factor / Size / Weight
MONSOON within NOAO ETS Project Life Cycle

1) Concept Definition Phase
2) Proposal Phase
3) Conceptual Design Phase (Here Now)
4) Preliminary Design Phase
5) Critical Design Phase
6) Implementation Phase
7) Delivery/Installation Phase
8) Evaluation Phase
9) On Going Support Phase

FOR MORE INFO...

ETS Standard Practice “Project Account Code System”
MONSOON as “Remote Image Server”

- Integrated Systems Concept:
  - Image Acquisition System vs “Controller”
    - Key Element in “Observatory” System
    - More than “Interface Electronics”
    - Focus on All Issues: Acquisition, Data Flow, Processing and Management
    - Remote Location / Reliability is of Vital Importance

- MONSOON Priority: Observing Efficiency
  - Maximize “Open Shutter” Integration Time !!!!
    - While providing Detector-Limited Performance
Fundamental System Design Issues

- "Detector-Limited" System Performance
  - For All Current & Anticipated Devices
- Physical Size and Form Factor Issues
- Power Dissipation & Cooling Near the Telescope
- System Assembly, Test, and Integration Time
- Reliability/Calibration/Data Integrity Issues
- Total Cost of Ownership
Universal Detector Acquisition System

- !!! Not Universal Controller !!!

- How Can this be Achieved?
  - (or is this the Continued Search for the Grail…)
    - Top Down Design Methodology
    - Modular Design,
      - Can Be Configured for Specific Application
    - Scalable Architecture
      - Based on Cost/Performance Criteria
    - Use “What’s Common to All” to Establish Framework
      - Standard Interface from “Bits to FITS”
    - Defined Interface Boundaries and Rational Architecture
MONSOON Scalable at Multiple Levels

1) Controller Level:
   Data Acquisition Hi-Speed “Standard” Backplane Based-Design,
   Acq Channels & Functionality Added as Needed to Support Multiple Devices / Controller
   Adapt to FPA Requirements…. Analog FPA => Digital FPA…. No Problem!

2) Fiber Optic Link Level:
   Upgraded from 1 GHz to 2.4GHz to Support Req’d Pixel Rate (50Mpix/s =>120Mpix/s)

3) Data Acquisition PC Level:
   PC’s Can Be Upgraded for Data Processing Req’s (CPU’s, Memory, Network Int)

4) Data Processing / Fiber Network Level:
   Systran Supports Data Broadcast Capability to Support Distributed Pixel Processing

5) System Level
   Controller/Data Acquisition Nodes Can be Added to Support Arbitrarily Large Systems
MONSOON Designed to Be Built Quickly, Efficiently, Effectively

- Heavy Use of COTS Technology
- Architecture Supports Distributed Parallel Development by Multiple Engineering Groups
- Use of Technologies and Tools Which are Available at Modest or No-Cost Now!
- Clear Definition of Interfaces and Subsystems
  - (Hardware & Software)
- Attention to Fundamental System Design Rules and a The Fundamental Laws of Physics as Applied to Electronic Systems
MONSOON System Hardware Architecture
MONSOON System Communications
(3 Critical Networks)

1) 1 GHz (2.4GHz) COTS Fiberoptic Network
   - Hi-Speed, Lo-Latency
   - 50Mpixel/s SL100, 120Mpixel/s SL240
   - Handles All Primary Communication to Controller Node
     - Command/Response & Pixel Data
   - Supports Point-to-Point, Loop, and Broadcast Topologies

2) Ethernet
   - Provides “Backdoor” Path for System Error Recovery, Diagnostics, and Development When Fiber Not Active
   - Not Intended for Any “Normal Mode” Use.

3) Controller Synchronization
   - Key System Element, “Hard-Synchronized” Controllers
   - Distributed 40MHz Master System Clock and Sync Pulse
   - Controlled Impedance, Skew Adjusted LVDS Signal Distribution
   - Skew Adjustable to <ns by Embedded CPU
MONSOON Key Technologies

- **Low-Cost “GHz – Class” PC’s**
  - Removes the Need for Embedded DSPs in System, (PC Cost ~ 2.5K)

- **Scalable Commercial High-Bandwidth FiberOptic Networks**
  - Buy not Build, Use a Well-Supported Commercial Product
    - Systran FiberExtreme SL100/SL240
      - SL100: 100MByte/s => 50Mpix/s, SL240 240MByte/s => 120Mpix/s

- **Standard Software Systems**
  - Use Dependable Components with Large User Base
    - Redhat LINUX
    - National Instruments LabView
    - SOAR NOAO Arcview (Under Evaluation Since 1/01)

- **State-of-the Art Analog & Mixed Signal Electronic Components**
  - Increased Performance with Reduced Power, Size, and Cost
    - Allows Construction of Large Channel Count Systems
Low-Cost “GHz – Class” PC’s

- Actual NOAO Benchmarks Published at IPAC Meeting on 4/01:
  - 10Hz Rates for Coadditions on 2k x 2k Images
  - > 2Hz Rates Projected on 4k x 4k Images

- Benchmarks taken with Low-Cost (~2.5k) Modest Performance Dell 800MHz Dual CPU PowerEdge 1400 Series Workstation

<table>
<thead>
<tr>
<th>TEST</th>
<th>IMAGE SIZE</th>
<th>LINUX PC Frames/S (Mpix/S)</th>
<th>SPARC ULTRA5 Frames/S (Mpix/S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coadd (1CPU, No Optimization)</td>
<td>2K x 2K</td>
<td>6.1 (24.2)</td>
<td>2.25 (9.0)</td>
</tr>
<tr>
<td>Coadd (2CPU, 2 Processes)</td>
<td>2K x 2K</td>
<td><strong>10.5</strong> (42)</td>
<td>N/A</td>
</tr>
<tr>
<td>Save FITS (1CPU, No Optimization)</td>
<td>2K x 2K</td>
<td>0.6 (2.3)</td>
<td>0.2 (.76)</td>
</tr>
<tr>
<td>Save FITS (2CPU, 2 Processes)</td>
<td>2K x 2K</td>
<td>0.6 (2.3)</td>
<td>N/A</td>
</tr>
</tbody>
</table>
SYSTRAN FiberExtreme

– Embedded “CMC” Daughter Card ↔ PCI Board System Components
– Multiple Network Topologies: Point to Point, Loop, Broadcast…
– May Be Widely Embraced in Astronomy (ACCORD, IRTF, Rockwell, etc.)
– NOAO Benchmark (8/01) Systran SL100 between two Dell PC’s
  • 100Mbytes/s (50Mpixel/s) sustained xfer rates for 4k x 4k images
MONSOON Advanced Mixed-Signal & Analog Components

- Development Driven by Telecommunications Industry
- 1/10 the Cost, 1/10 the Size, 1/10 the Power of Previous Generation Hybrid ADC Technologies Used in SDSU-II and Redstar 2 & 3 Systems

Redstar 2 & 3

SDSU-II

- Multiple Devices have been Prototyped and Evaluated Already at NOAO (1/01, to 9/01)
Electronics – Signal Chain

- SDSU II Dual Channel Video Board
  - 2 channels
  - 1 Mpixel/sec
  - CDS, 16 bit ADC
  - 15 W power

- Analog Devices 9826
  - 3 channels (RGB)
  - 15 Mpixel/sec
  - CDS, 16 bit ADC
  - 400 mW power
**MONSOON Performance Metrics**

- All Data Pipelines Support to 32-bit Transfer for Future Expansion
- Current Dynamic Range: > 60,000:1
  - 16-Bit 1MHz ADC Resolution, supporting S/N > 90dB
- NonLinearity: < 0.1% over Entire Range
- ReadNoise: < 10% Contribution to Total System Readnoise
  - Actual Input Noise and System Gain & Bandwidth Set By FPA Used
- Channel to Channel Crosstalk: < 0.005%
- Pixel to Pixel Crosstalk: < 0.01%
- Data Rates: Upto 120Mpixel/sec per Controller Chassis
- Data Processing Rates: Unlimitted with Fiber Broadcast Capability
- # of Channels/Controller: Upto 256 Channels per Controller Chassis
- # of Controllers/System: >100
- Calibrated, Measured, Recorded Performance.
MONSOON 3 Board / 3 Bus System

- **3 Boards**
  - 1) Master Control Board (MCB)
    - Common to All Monsoon Systems
  - 2) Clock & Bias Board (C&B)
    - Designed to Meet FPA Needs
    - 2 or More Versions Planned (IR & CCD)
  - 3) Acquisition Board
    - Designed to Meet FPA Needs
    - 2 or More Versions Planned (IR & CCD)

- **3 Buses**
  - 1) 64-Bit Pixel Bus
    - HiBandwidth Synchronous Transfer of Pixel Data from Acq Board to MCB
  - 2) Sequencer Bus
    - Hi Speed Synch Timing Bus (MCB to Acq & C&B Boards) for All Controller Data Timing Functions
  - 3) Serial Configuration Bus
    - 3 Wire Serial Configuration Bus to Configure & Readback Acq/C&B Boards
MONSOON Controller Packaging

- 6U Eurocard Format
- CPCI Digital Backplane
- Custom Analog Backplane
CPCI Digital Backplane

- COTS Product “Buy Today not Build Tomorrow”
- Avoid Unnecessary Overhead from PCI Bus Protocol with “Simple” 3 Bus Data Path Definition.
- Use 64-Bit Pixel Bus for > 120M Pixel/S Xfer Rate
- Use PCI “Reflected Wave” Methodology
- Controlled Z, Hi-Speed Environment
System Specific Analog Backplane

- Rigid-Flex Technology
- Place All OverVoltage, ESD Protection & Filtering Circuitry as Close to the Focal Plane as Possible to Best Protect Devices
- New 3-D Solid Models Give Necessary Detail for Accurate Layouts
- Almost All New FPAs and CCDs Have Flex Circuit Interconnects
- Cost Same as PCB, Not an Issue
Master Control Board

- Provides All Timing & Sequencing to System
  - Provides Monsoon System Clock Networking
  - Employs FPGA (Xilinx Vertex) Hardware Sequencer
    - 300K Gate Density, Embedded Ram, Reconfigurable
- Provides Interface to Systran Fiber
  - Fiber Handles All Primary Cmd/Response and Pixel Data
- Provides Interface to Embedded Ethernet Processor
  - Ethernet Used for System Configuration and “Back-Door” Reset
  - Processor Used for System Configuration, Housekeeping & Integration Timing
  - Does Not Generate Waveforms or Touch Pixel Data
Embedded Ethernet Core Processor

Rabbit RCM2100
10-Base T Ethernet & TCP/IP Ready
20MHz CPU, 512k Ram, 512k Flash
$279 Development System
<$100 Board Price
Systran SL100 Interface

- Mechanical - Simple Embedded Daughter Board
- Electrical - Front Panel Data Port
  - Simple “Industry Standard” 32-bit Parallel w/Handshaking
Front Panel Data Port Specifications
VITA 17-199x
Rev. 1.7
November 24, 1998

Sponsored by the
VITA Standards Organization (VSO)

This is an unapproved specification.
Do not specify or claim conformance to this document.

Abstract
This standard provides a specification of the protocol and mechanical characteristics of the Front Panel Data Port. This extension to the VME standard consists of a multidrop synchronous parallel non-addressable bus connection between multiple boards in a single chassis. The connection is made to a connector on the front panel of each board by means of an eighty conductor ribbon cable.

Serial Front Panel Data Port (FPDP) Draft Standard
VITA 17.1 - 199x

Draft 0.5
February 26, 2001

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VSO is the Public Domain Administrator of this draft standard and guards the contents from change except by sanctioned meetings of the task group under due process.

VITA Standards Organization
7825 East Gelding Drive, Suite 104
Scottsdale, AZ 85260
Ph: 602-951-8866 Fx: 602-951-0720
URL: http://www.vita.com
System Synchronization

- Distributed 40 MHz Clock and Synch Signal
- LVDS Signaling, TWSP Cable, Terminated “Skew Compensated” Lines
- System “Hard Synched” to ns Timing
- Synch Signal Can be Used to Synch Controllers to Each Other or External Source Such as Time Source, Chop Signal, AO System…
- Synch Signal is Really Serial Input Line, Can Be Extended to Many Uses.
Clock & Bias Board Model

- Board May be Tailored to FPA & System Req’s
- All Interface to MONSOON Bus Through FPGA or CPLD
  - This Allows:
    - 1) Reconfiguration of Bus Interface Signals if Needed
    - 2) PCI Compatible Signals
    - 3) Room for Added Functionality & Lots of Flexibility
- All Clock Voltages & Bias Voltages Will Have Readback Capability
- Most Bias Voltages & Clock Rails Set by the Serial Cfg Bus
  - ORION Clock & Bias Board Will Support High-Speed Parallel DACs for Critical Nodes
- Similar Advances in CMOS DACs Allow Single Board to have 10’s to 100’s of Channels on 6U Format
Possible Clock & Bias Board

- QTY 4 EL7457C Quad Drvr
- QTY 1 8 Channel 12-Bit DAC
- QTY 1 12 Channel 12-Bit DAC
- 16 TTL Clock Channels for Mux Select
- Bilevel Clock Channels in Groups of 4
- 16 CLK
- 3 CTL
- 16 CLK
- DAC
- ADC
- Monsoon Bus Interface Logic
- DAC Interface Logic
- Local Pattern Generator (if req’d)

12/8/2006
Acquisition Board Model

- All Interface to MONSOON Bus Through FPGA or CPLD
  - This Allows:
    - 1) Reconfiguration of Bus Interface Signals if Needed
    - 2) Room for Added Functionality
      - (Digital Averaging, Dynamic Gain Select)
    - 3) PCI Compatible Signals
- All Bias and Offset Voltages Will Have Readback Capability
- Channels Counts of 16 to 32 to ??? on 6U Format
12-Channel Acquisition Circuitry

3 Channel AFE
- CDS
- PGA
- 16-BIT ADC

ACQ CPLD
- PIXEL DATA PROCESSING LOGIC
- DATA INTERFACE LOGIC
- AFE CLOCKING LOGIC
- AFE CFG INTERFACE LOGIC

AFE CFG

FROM CCD OUTPUTS

12 VIDEO ACQUISITION CHANNELS

64 PIXEL DATA BUS

SEQUENCER BUS

SERIAL CFG BUS

AFE CONFIGURATION FROM SERIAL CFG BUS (FROM RABBIT RCM MODULE)
Potential Pixel Processing at the CPLD Level

- Dynamic Gain Selection “On The Fly” Based on Pixel Data
- Raises Effective Number of ADC Bits to ????
MONSOON
System Implementations
NEWFIRM
Analog FPA System Diagram
NEWFIRM
Digital FPA System Diagram
MONSOON for NEWFIRM
QUOTA Detector Details – Orthogonal Transfer

- Orthogonal Transfer
  - remove image motion
  - high speed (few usec)

Normal guiding (0.73")  OT tracking (0.50")
Four OTA served by an Interface Unit and Gbit fiber
- Decodes computer commands
- Synchronizes readout
- Formats data for computer transmission

64 Mpixel = 128 Mb
QUOTA to ODI System Scaling

SCALABLE DATA ACQUISITION SYSTEM ARCHITECTURE

QUOTA (ODI = 16x)
QUOTA Software Tasks

- Observation shift and guide loop

1. Open shutter
2. Integrate 10-100 msec
3. Read out guide star patch
4. Centroid guide star
5. Apply shift to OT image
6. Exposure done?
   No... then go to 2.
7. Yes. Close shutter
8. Read out entire science array.
MONSOON
System Software Architecture

Nick Buchholz
What Is ArcVIEW?

- LabVIEW based array controller system
- Developed by Imaginatics for SOAR
- Not ruled out as an option
- Needs more study
MONSOON Current Status

- System Design has Been in Process Since 12/00.
- Software Design has Been in Process Since Spring of ‘01
- All Key Hardware Technologies ID’d & Prototyped at Component Level.
- Key Software Technologies ID’d & Evaluated (Exception Arcview)
- 12 Channel CCD Prototype Currently In Board Fabrication,
  - Initial Assembly and Test Complete by 12/1/01
- 64 Channel IR Prototype Currently In Layout.
  - Prototype Master Control Board
  - Prototype 16+ Channel IR Acquisition Board
- MONSOON CoDR now 10/29/01
MONSOON CCDPrototype

- 12-CHANNEL 16-BIT > 1MHZ ACQUISITION
  - PREAMP/CDS/ADC, 1/2/4/8/16 SAMPLE DIGITAL AVERAGING
- 12-CHANNEL HI VOLTAGE LOW-NOISE BIAS
  - +/-40V RANGE, 12-BIT RESOLUTION, ANALOG READBACK
- 12-CHANNEL LO VOLTAGE LOW-NOISE BIAS
  - +/-12V RANGE, 12-BIT RESOLUTION, ANALOG READBACK
- 24-CHANNEL CLOCK DRIVER
  - +/-12V RANGE, 12-BIT RESOLUTION, ANALOG READBACK
- CPLD CLOCK PATTERN GENERATOR
- 50 MPIXEL/SEC BIDIRECTIONAL FIBERLINK
  - 1Gb/S FIBER UPGRADEABLE TO 2.4Gb/S
- 20MHZ EMBEDDED PROCESSOR
  - 10Mb/S ETHERNET LINK, TCP-IP STACK
- SINGLE BOARD 6U EUROCARD (VME) FORM FACTOR
CCD Prototype Goals

- Further Evaluate:
  - Key Technologies
    - SL100 Fiber
    - Rabbit RCM2100 Embedded
    - AD9826 AFE
    - Opamps
    - CCD Clock Drivers
    - CPLDs
  - Component Packaging Densities
  - Power Consumption Issues
  - Controller Synchronization Issues
- If Prototype Successful:
  - LBNL MiniMosaic
  - Orthogonal Transfer CCD Evaluation Camera
CCD Prototype Layout
Multiple Engineering Groups Can Develop in Parallel

- System Design Using COTS Fiber and CPCI Backplane Means Development Starts Now
- Modular Hardware Design With Well-Defined Interface Means Different Clock & Bias Boards or Acquisition Boards Can Be Developed Simultaneously
- FPGA Based Bus Interface Gives Added Flexibility in Implementation.
- Use of Low-Cost Components and Tools Allows Minimal Investment to Participate in Design Effort
- Break the Sequential Software Development Effort
System Design Allows Immediate Software Development
MONSOON Project Plan Milestones

- Attend ACCORD Controller Workshop 11/6/01
  - at Lick Obs to Promote Collaborative Effort
- MONSOON PDR in 1/02
- MONSOON CDR in 3/02
- MONSOON Subassembly Fabrication Complete by 6/02
- Initial MONSOON System Integration Complete in 8/02
- Initial System Software Complete 9/02
MONSOON
Estimated Development Costs

- Estimate 3.5 FTE over Fiscal 2002
- Staffing Plans
  - NOAO Tucson Staff
    - Detector R&D Group Staff (1.0-2.0)
    - Nick Buchholz (0.75) / Phil Daly (0.25) Software
    - Dee Stover PCB Layout, Documentation (0.5)
    - UofA Engineering Interns (0.5 Eq FTE EE, 0.5 Eq FTE Software)
    - Margin - Outside Consultants (FPGA Design, Embedded Software)
  - CTIO Staff ???
    - Ricardo Schmidt, Michael Warner, Gustavo, Eduardo
  - ArcView (Would Potentially Reduce Software Drastically) ????
  - Outside Collaborators (ACCORD) ????
MONSOON
Estimated Capital Expenditures

- 3 Development Platforms Already In House
  - Dell PowerEdge PCs with GHz CPU & 512MByte RAM
  - Systran SL100 Links (PCI to CMC)
- All Components for CCD Prototype Purchased and Received
- 75% of IR Prototype Components Purchased and Received
- Estimated Outstanding Capital Expenditures (90K)
  - Components (25K)
  - PCB Assemblies (15K)
  - Equipment/Software (20K)
  - Outside Consultants (30K)
MONSOON
Estimated Fabrication Costs

- ORION 64 Channel System
  - 70k
- NEWFIRM 128 Channel System
  - 102K
- QUOTA 32 Channel System *
  - 70k
- ODI 512 Channel System *
  - 1M

* Likely to Require Repackaging for WIYN Mechanical Requirements