Gemini Near Infrared Coronagraphic Imager
Electronics System Document
GEMINI SDN3001

MKIR# NICI –900-200-01
Rev 0.1 (prerelease)
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Table of Contents

1 Gemini Near Infrared Coronagraphic Imager Electronics System Document

1.1 Overview

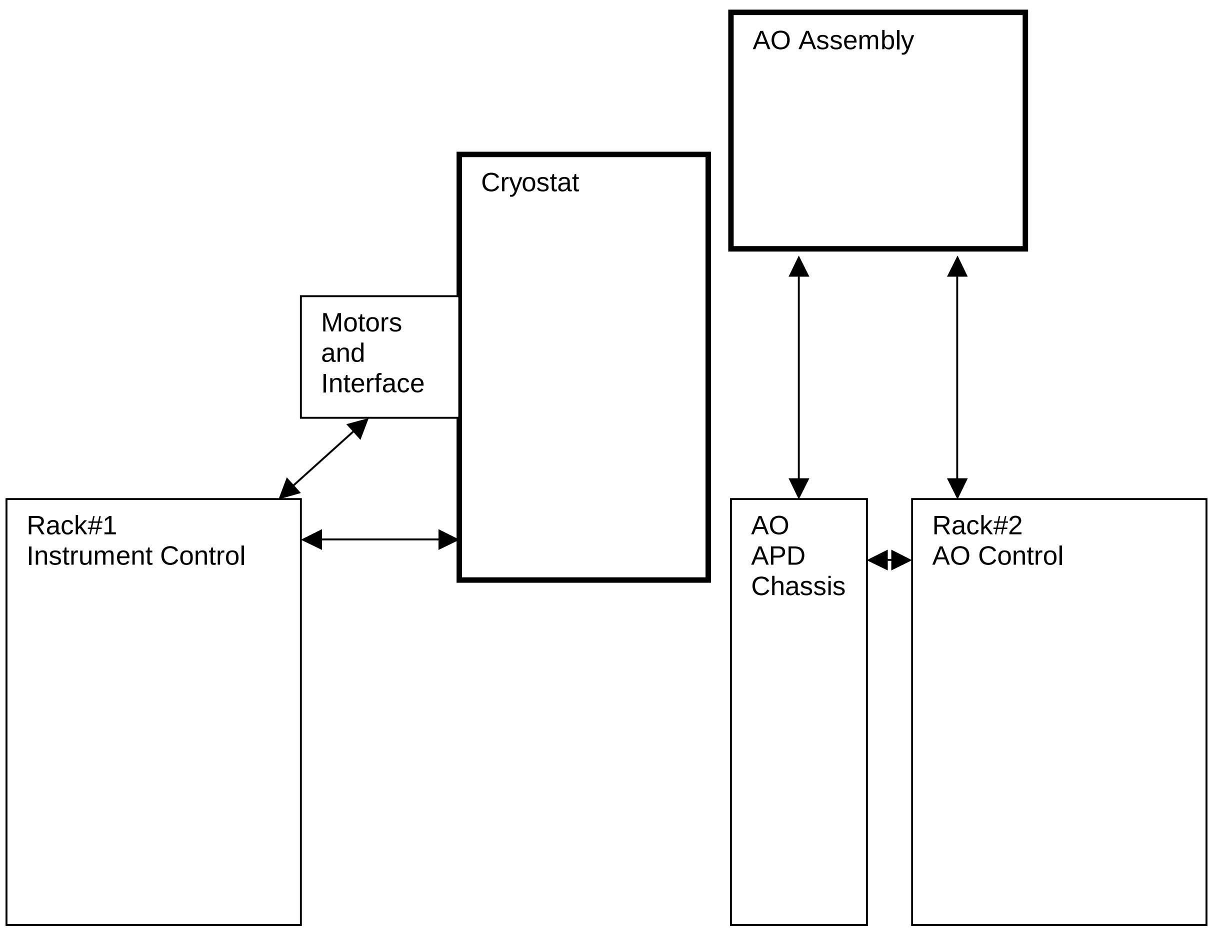
1.1.1 Purpose

This document details the electronics system level description for the Gemini Near Infrared Coronagraphic Imager, NICI. The document provides the highest level starting point for information regarding all electronics subsystems in NICI.

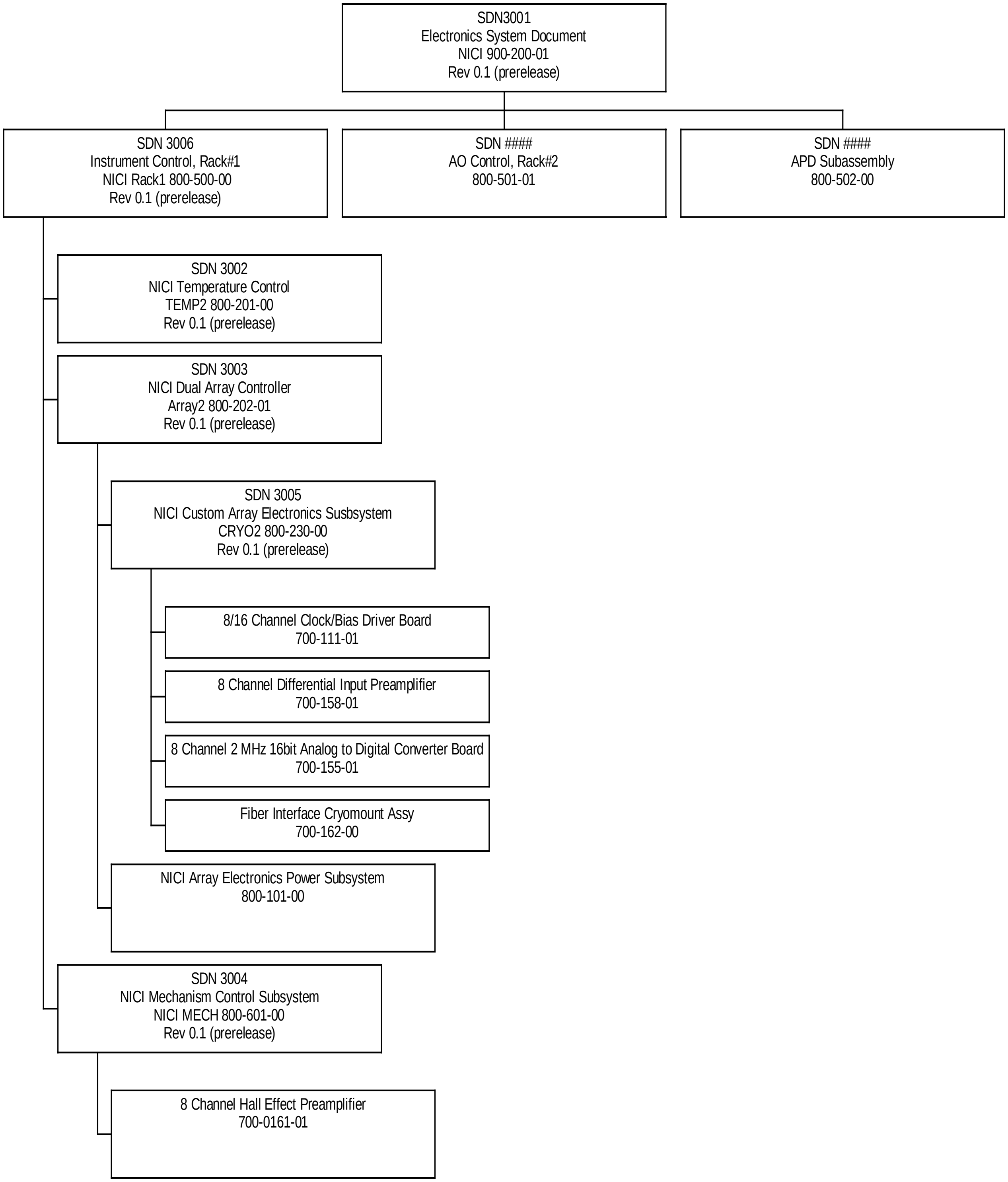
1.1.2 Major Assemblies

The major subsystems for NICI are physically located in two Gemini standard 1.3 meter cooled electronics racks, the AO assembly, AO APD chassis and cryostat mounted assemblies.

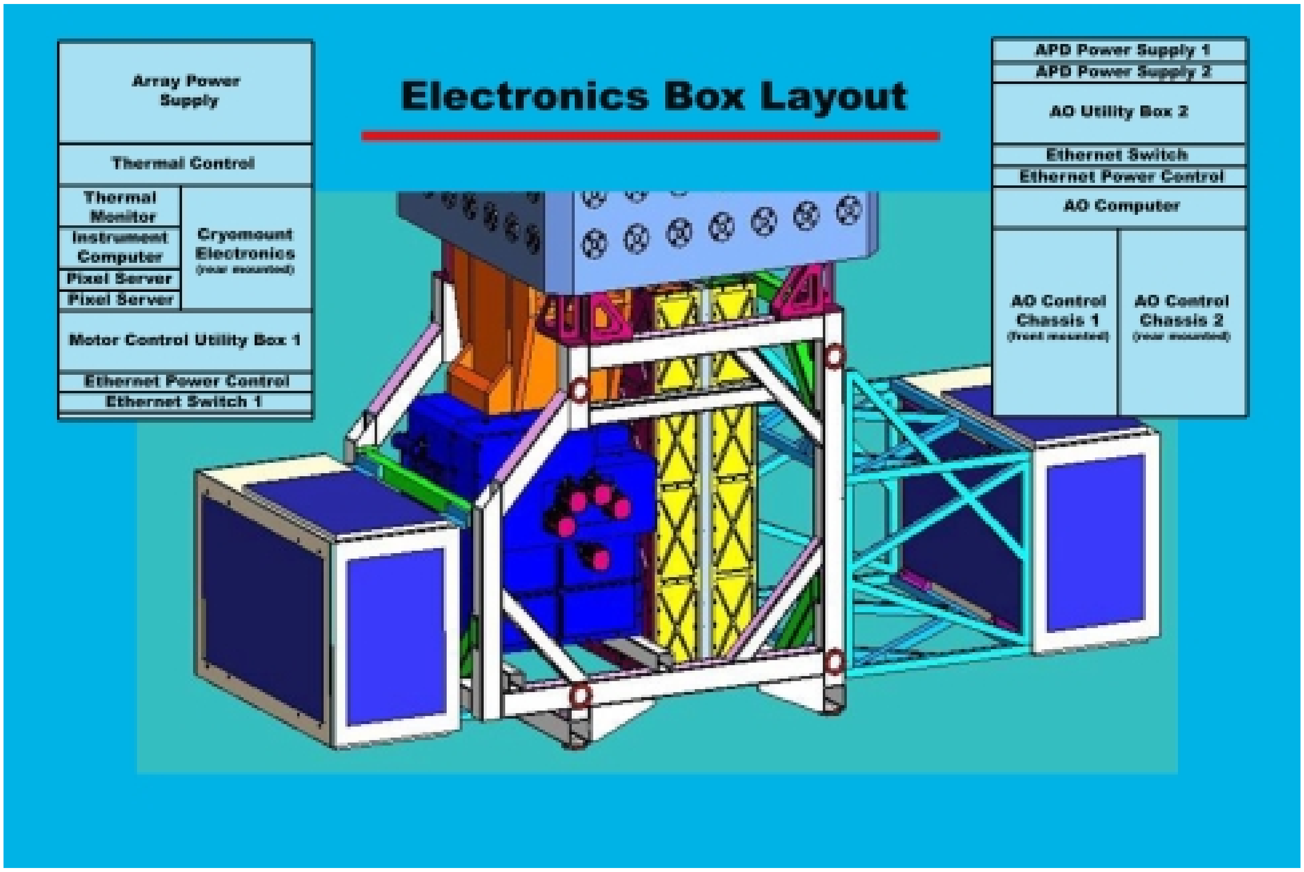
1.1.3 Block Diagram



1.1.4 Subsystem Document Tree



1.1.5 System Layout Diagram



1.1.6 System Power Totals

The estimated electronics system total power dissipation is 2861 Watts.

1.2 Instrument Control, Rack#1

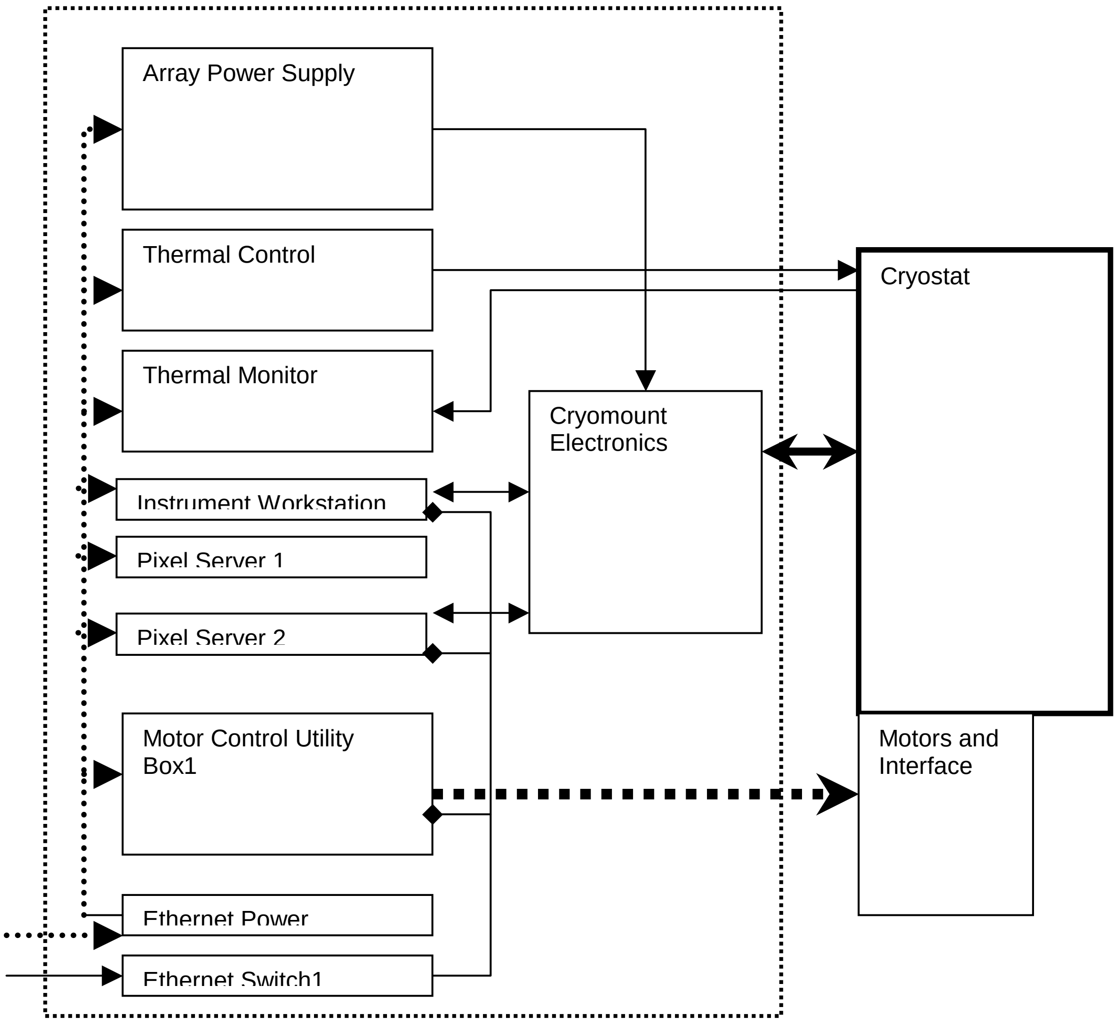
1.2.1 Functional Description

Rack #1 houses the majority of the NICI camera and motor control electronics. The functions of the dual array drive and readout, cryogenic thermal control, monitoring and mechanism control are housed in major subsystems in this rack. Major interfaces are made to the cryostat and cryostat mounted motor systems.

1.2.2 Reference Documents

NICI Instrument Control Rack#1 800-500-00

1.2.3 Block Diagram



1.2.4 Mechanical Dimensions

The 1.3 meter rack external dimensions.

External Height	Inches	Meters	External Width	Inches	Meters	External Depth	Inches	Meters
		1300mm						

The 1.3 meter rack internal dimensions.

Available front rack space	Inches	Meters	Available Width HP	Inches	Meters	Available Depth	Inches	Meters
22.5U	31.50in	800.10mm	84	16.75in	425.45mm		31.50in	800.10mm

1.2.5 Subassembly Mechanical Details

Assemblies										
Number	**Subassembly Name**	**Manufacturer's Part**	**Height (in)**	**Height (mm)**	**U**	**Width (in)**	**Width (mm)**	**HP**	**Depth (in)**	**Depth (mm)**
1	Instrument Workstation	Compaq Proliant DL360	1.65in	41.91mm	1	16.75in	425.45mm	84	16.75in	425.45mm
2	Pixel Server 1	Compaq Proliant DL360	1.65in	41.91mm	1	16.75in	425.45mm	84	16.75in	425.45mm
3	Pixel Server 2	Compaq Proliant DL360	1.65in	41.91mm	1	16.75in	425.45mm	84	16.75in	425.45mm
4	Array Power Supply	HP 66000	7.50in	190.50mm	5	16.75in	425.45mm	84	26.70in	678.18mm
5	Thermal Control	Lakeshore 332S X 2	3.50in	88.90mm	2	16.75in	425.45mm	84	22.75in	577.85mm
6	Thermal Monitor	Lakeshore 218	3.50in	88.90mm	2	16.75in	425.45mm	84	16.75in	425.45mm
7	Motor Control Utility Box1	Elma Type14 3U chassis	4.95in	125.73mm	3	16.75in	425.45mm	84	20.96in	532.38mm
8	Ethernet Power Control1	Baytech RPC3	1.65in	41.91mm	1	8.55in	217.17mm	43	5.25in	133.35mm
9	Ethernet Switch1	TBD	1.65in	41.91mm	1	16.75in	425.45mm	84	5.25in	133.35mm
10	Cryomount Electronics	MKIR	9.90in	251.46mm	6	16.75in	425.45mm	84	12.0in	304.80mm
				Rack#1	**24**					

1.2.6 Rack #1 subassembly physical positions

Rack #1 TOP DOWN LAYOUT				800.10mm available	
Number	**Subassembly Name**	**Manufacturer's Part**	**Height (in)**	**Height (mm)**	**U**
FRONT MOUNT					
4	Array Power Supply	HP 66000	7.50in	190.50mm	5
5	Thermal Control	Lakeshore 332S X 2	3.50in	88.90mm	2
COMBINED MOUNTING FRONT MOUNT					
6	Thermal Monitor	Lakeshore 218	1.65in	41.91mm	1
1	Instrument Workstation	Compaq Proliant DL360	1.65in	41.91mm	1
2	Pixel Server 1	Compaq Proliant DL360	1.65in	41.91mm	1
3	Pixel Server 2	Compaq Proliant DL360	3.30in	83.82mm	1
REAR MOUNT					
10	Cryomount Electronics	MKIR	9.90in	251.46mm	6*
FRONT MOUNT					
7	Motor Control Utility Box1	Elma Type14 3U chassis	4.95in	125.73mm	3
8	Ethernet Power Control1	Baytech RPC3	1.65in	41.91mm	1
9	Ethernet Switch1	TBD	1.65in	41.91mm	1
				front subtotal	18

1.2.7 Power Dissipation Estimates

See the supporting subsystem documents for a more detailed breakdown.

Subassembly Name	Power	Voltage input	Current input
Pixel Server 1	330.0W	120.0VAC	3.89A
Pixel Server 2	330.0W	120.0VAC	3.89A
Array Power Supply	91.8W	120.0VAC	.54A
Thermal Control	339.4W	120.0VAC	2.0A
Thermal Monitor	25.5W	120.0VAC	.15A
Motor Control Utility Box1	72.0W	120.0VAC	.85A
Ethernet Power Control1	5.0W	120.0VAC	.06A
Ethernet Switch1	5.0W	120.0VAC	.06A
Total	**1198.7W**		**11.43A**

1.2.8 Subassembly Weight Estimates

Subassembly Name	Weight (lbs)	Weight (kg)
Pixel Server 1	50.0lb	22.68kg
Pixel Server 2	50.0lb	22.68kg
Array Power Supply	69.0lb	31.30kg
Thermal Control	21.0lb	9.53kg
Thermal Monitor	6.6lb	2.99kg
Motor Control Utility Box1	30.0lb	13.61kg
Ethernet Power Control1	3.0lb	1.36kg
Ethernet Switch1	3.0lb	1.36kg
Cryomount Electronics	25.0lb	11.34kg
TOTAL	257.60lb	116.85kg

1.2.9 High Level Array Control System Functional Requirements

Must operate two 4 quadrant Aladdin type III style arrays
Reference Document: SDN 3003 NICI Dual Array Controller

Must allow synchronization of readouts of the two arrays to 1 millisecond.

'Quick Answer': The Clocking FPGA circuitry located on the FCRYO2 board will start exposures when in an ARM state and after receiving an optocoupled TTL level TRIGGER signal. Clocking will be synchronized to within 140nsec.
Reference Document: FCRYO2 700-2##-##

Single subarray mode minimum size 8x16 placed anywhere in the array and reflected to all four quadrants.
Global reset
Single sampled readout mode
Double correlated sampled readout mode
Multiple NDR noise reduction sampling mode
'Quick Answer': The Clocking FPGA circuitry located on the FCRYO2 board allows for flexible clocking encompassing these requirements. .
Reference Document: FCRYO2 700-2##-##

Connect to Gemini through a Socket for remote control
State set and state read commands
Populate the FITS header and ship the data to the DHS
Must operate in a standalone mode or under Gemini control in a remote mode
Must provide an image display in standalone mode
Must provide local storage for standalone mode
Reference Document: SDN 3003 NICI Dual Array Controller

Must time stamp frames using Gemini supplied time board*
'Quick Answer': NICI will use a MKIR supplied time board located in the Pixel Servers
Reference Document: SDN 3003 NICI Dual Array Controller
Must have macro capability in stand alone mode
Reference Document: SDN 3003 NICI Dual Array Controller

1.2.10 High Level Array Control System Performance Requirements

Read noise - the controller should not increase the device noise by more than 10%
'Quick Answer': 'The gain is fixed at X5 and the bandwidth is limited to ~2.9Mhz with resulting calculated noise (with a 1K souce impedance) is equal to 53.2uV. For the +/-2.5V input range of the ADCs' one bit (LSB) is equal to 76uV so the preamplifier contributes less than 1 LSB.'
Reference Document: PREAMP8 700-158-01
'Quick Answer': The previous generation array controllers using the same analog and ADC circuitry has been able to achieve the read noise requirement on 6 different Aladdin arrays on 3 different telescopes (SUBARU, IRTF, NRL/NO Flagstaff).
A/D resolution – adequate to get two bits on the noise
'Quick Answer': The gain is fixed at X5. From experience, the e/ADU ratio averages ~10e/ADU at this setting, leaving ~ 4bits of resolution on the noise from single Fowler pair readout of the Aladdin III.
Reference Document: PREAMP8 700-158-01
Full frame coadd rate - 2 Hz required (10 Hz goal)
Full frame to disk rate – 2 Hz required (10 Hz goal)
'Quick Answer': As of 3/15/2002, testing has that shown data processing and storage rates have achieved the 2 Hz requirement and 10Hz goal for both coaddition and storage.
Display frame rate stand alone mode – .5 sec to display frame desired.
'Quick Answer': As of 3/15/2002, no testing has been performed.

1.3 AO Control, Rack#2

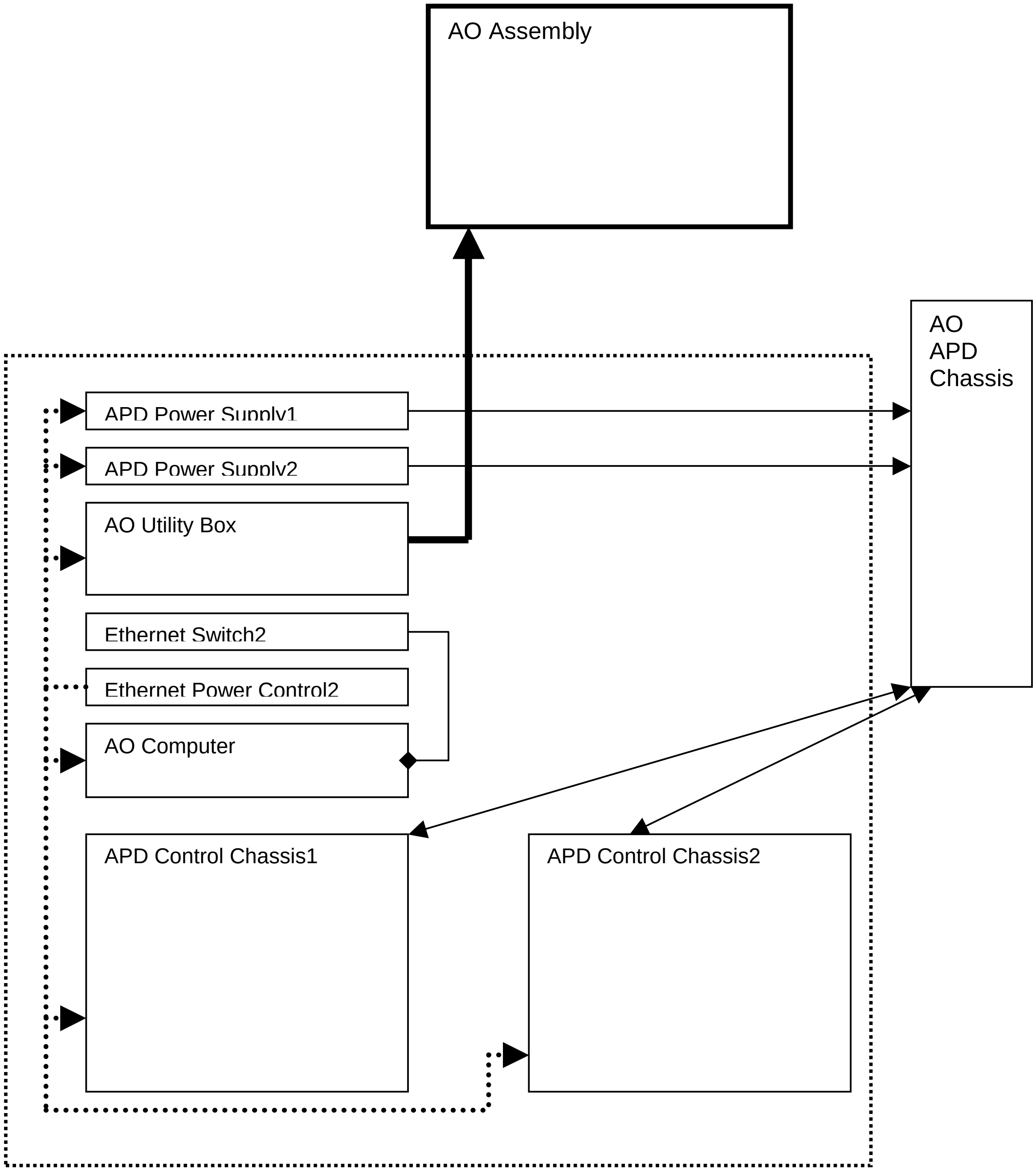
1.3.1 Functional Description

Rack #2 houses the majority of the AO control electronics. The functions of APD power supply , APD output counting,membrane and deformable mirror drive are housed in major subsystems in this rack. Major interfaces are made to the AO assembly and APD chassis.

1.3.2 Reference Documents

800-501-01 NICI Rack #2 Document

1.3.3 Block Diagram



1.3.4 Mechanical Dimensions

The 1.3 meter rack external dimensions.

External Height	Inches	Meters	External Width	Inches	Meters	External Depth	Inches	Meters
		1300mm						

The 1.3 meter rack internal dimensions.

Available front rack space	Inches	Meters	Available Width HP	Inches	Meters	Available Depth	Inches	Meters
22.5U	31.50in	800.10mm	84	16.75in	425.45mm		31.50in	800.10mm

1.3.5 Subassembly Mechanical Details

Number	Subassembly Name	Manufacturer's Part	Height (in)	Height (mm)	U	Width (in)	Width (mm)	HP	Depth (in)	Depth (mm)
10	Ethernet Switch2	TBD	1.65in	41.91mm	1	16.75in	425.45mm	84	5.25in	133.35mm
11	Ethernet Power Control2	Baytech RPC3	1.65in	41.91mm	1	8.55in	217.17mm	43	5.25in	133.35mm
12	AO Computer	Dell Powedge 2550	3.30in	83.82mm	2	16.75in	425.45mm	84	16.75in	425.45mm
13	AO Utility Box2	Elma Type14 3U chassis	4.95in	125.73mm	3	16.75in	425.45mm	84	20.96in	532.38mm
14	AO Control Chassis1	Elma Type12 8U chassis	14.0in	355.60mm	8	16.75in	425.45mm	84	19.60in	497.84mm
15	AO Control Chassis2	Elma Type12 8U chassis	14.0in	355.60mm	8	16.75in	425.45mm	84	19.60in	497.84mm
16	APD power Supply1	Sorenson DCS8-125E	1.65in	41.91mm	1	16.75in	425.45mm	84	19.0in	482.60mm
17	APD power Supply1	Sorenson DCS8-125E	1.65in	41.91mm	1	16.75in	425.45mm	84	19.0in	482.60mm

1.3.6 Rack #2 subassembly physical positions

Rack #2 TOP DOWN LAYOUT

Number	Subassembly Name	Manufacturer's Part	Height (in)	Height (mm)	U
FRONT MOUNT					
16	APD power Supply1	Sorenson DCS8-125E	1.65in	41.91mm	1
17	APD power Supply1	Sorenson DCS8-125E	1.65in	41.91mm	1
13	AO Utility Box2	Elma Type14 3U chassis	4.95in	125.73mm	3
10	Ethernet Switch2	TBD	1.65in	41.91mm	1
11	Ethernet Power Control2	Baytech RPC3	1.65in	41.91mm	1
				subtotal	7
COMBINED MOUNTING FRONT MOUNT					
12	AO Computer	Dell Powedge 2550	3.30in	83.82mm	2
14	AO Control Chassis1	Elma Type12 8U chassis	14.0in	355.60mm	8
				front subtotal	17
REAR MOUNT					
15	AO Control Chassis2	Elma Type12 8U chassis	14.0in	355.60mm	8

1.3.7 Power Dissipation Estimates

See the supporting subsystem documents for a more detailed breakdown.

Subassembly Name	Power	Voltage input	Current input
Ethernet Switch2	5.0W	120.0VAC	.06A
Ethernet Power Control2	5.0W	120.0VAC	.06A
AO Computer	330.0W	120.0VAC	3.89A
AO Utility Box2	72.0W	120.0VAC	.85A
AO Control Chassis1	200.0W	120.0VAC	2.36A
AO Control Chassis2	200.0W	120.0VAC	2.36A
APD power Supply1	90.0W	120.0VAC	.53A
APD power Supply1	90.0W	120.0VAC	.53A
	992.0W		

1.3.8 Subassembly Weight Estimates

Subassembly Name	Weight (lbs)	Weight (kg)
Ethernet Switch2	3.0lb	1.36kg
Ethernet Power Control2	3.0lb	1.36kg
AO Computer	50.0lb	22.68kg
AO Utility Box2	30.0lb	13.61kg
AO Control Chassis1	25.0lb	11.34kg
AO Control Chassis2	25.0lb	11.34kg
APD power Supply1	19.0lb	8.62kg
APD power Supply1	19.0lb	8.62kg
Ethernet Switch2	174.0lb	78.93kg
TOTAL	3.0lb	1.36kg

1.4 System Grounding

1.4.1 Plan Description

The grounding plan for the instrument is handled at five levels. The first is at the cryostat mounted electronics level. Separate analog and digital ground planes are used on all of the cryostat electronics boards and the backplane. A single point connection between them is unavoidably made at the analog to digital converters because the devices themselves are manufactured with an internal connection between the two potentials. The fact that there are multiple ADCs in the system places the best point for a single point ground at these connection points. This configuration dictates that the power supplies must have floating outputs. Previous experience has shown that there can also be substantial coupling capacitance between the power supply chassis and the outputs, so isolation is also often necessary.

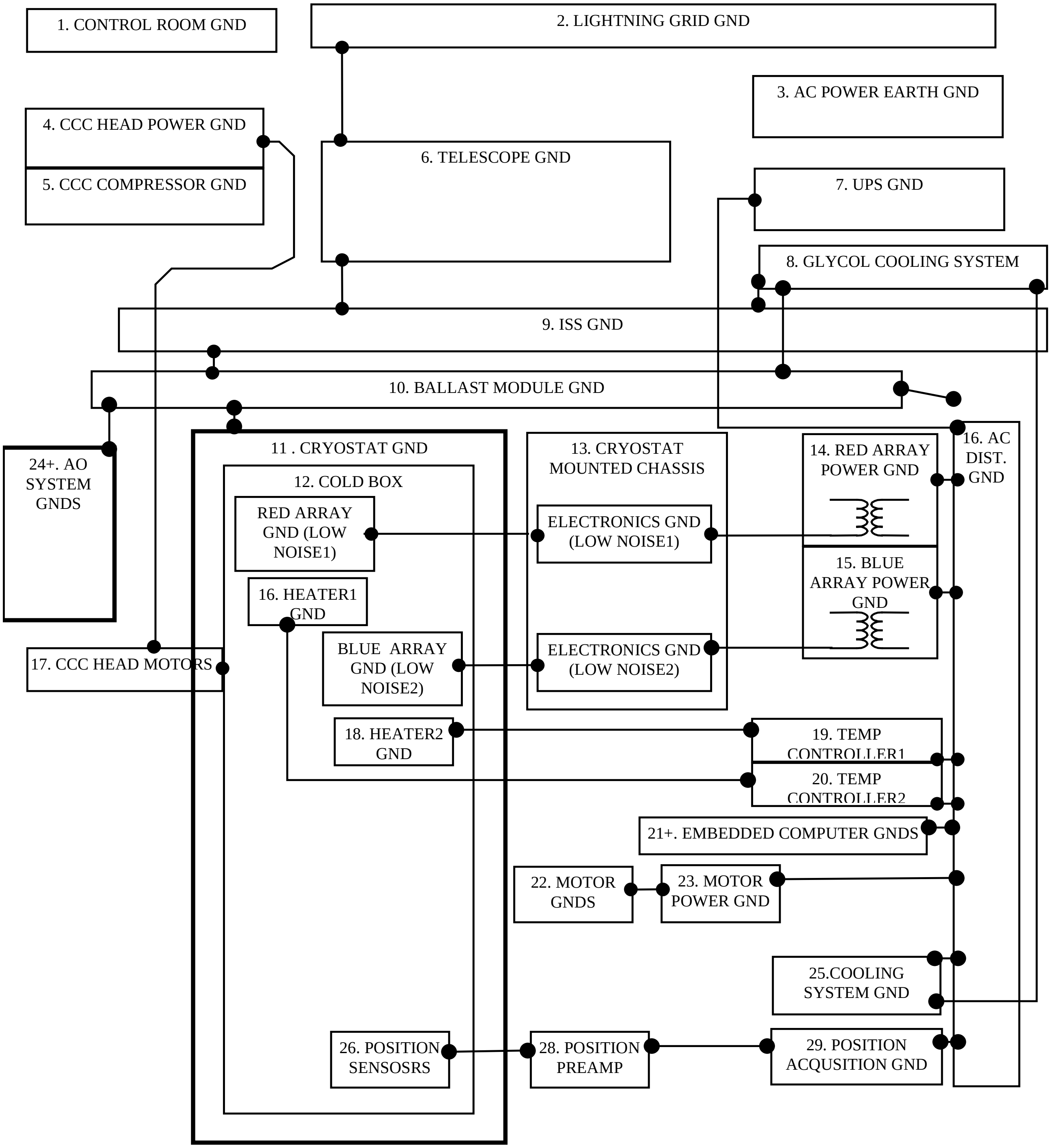
The second level of grounding is accomplished with the fiber optic link between the Embedded Computers (Instrument Workstation and Pixel Servers) and the cryostat mounted electronics. This complete optical isolation is intended to keep the high current and high frequency power distortion generated by the computer systems away from the low noise array electronics.

Each array electronics subsystem will have its own independent ground (that can be alternatively shorted to the other). This third level of grounding is intended to minimize crosstalk between the readout of the two arrays. The dual independent power supply systems support this configuration.

Another area of concern is the fourth level of ground isolation that between the closed cycle cooler system and the cryostat mounted electronics. The closed cycle cooler will not be electrically isolated from the cryostat vacuum jacket, so the two array wiring inside will be isolated.

The fifth level of the system grounding plan is illustrated in the following figure. It is an attempt to identify all of the different ground potential points in the facility that may affect the performance of the instrument. The diagram provides a starting point to identify and fix grounding problems.

1.4.2 System Ground Diagram



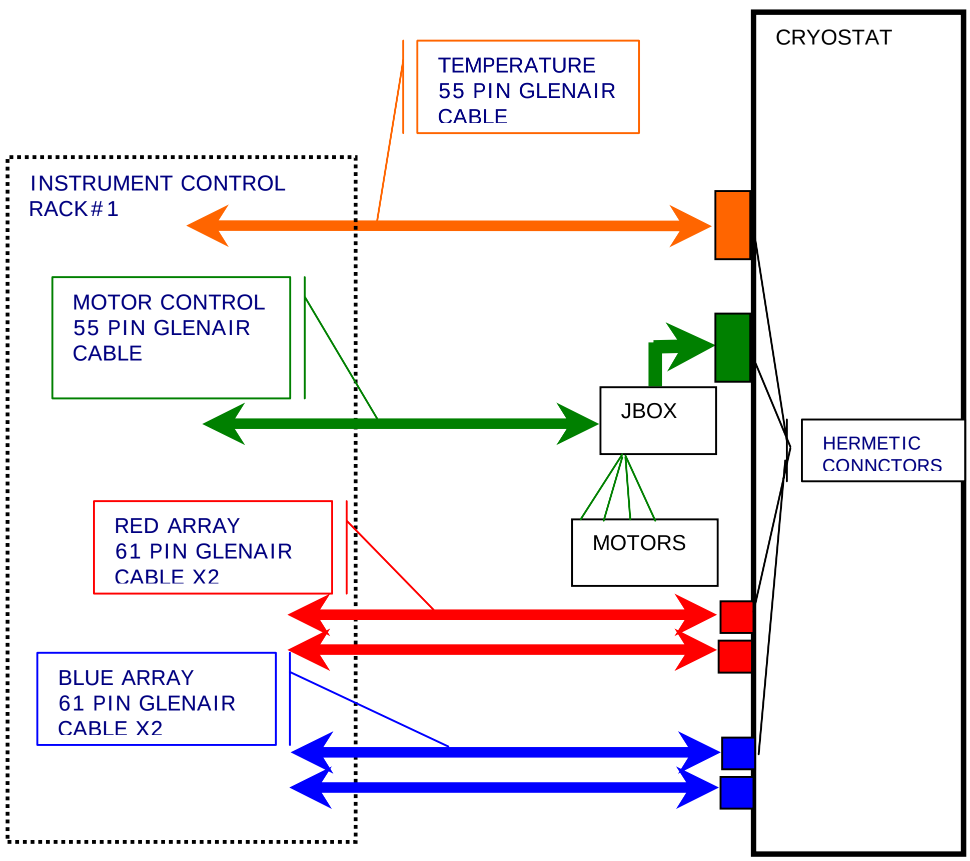
1.5 Connections and Cabling

1.5.1 Rack#1 to Cryostat External Cabling

Four types of connections are made between Rack#1 and the Cryostat Assembly. There are a total of 8 cables.

Type	Qty	Name	Manufacturer's Part	# conductors	Type of signals	Length	Connectors
1	1	Temperature Cable	Glenair 55pin	55	Low level/noise and heater power	15ft	cylindrical
2	1	Motor Control Cable	Glenair 55pin	55	Low level/noise and 48VDC	15ft	cylindrical
3	4	Array Cables	Glenair 61 pin ABC56145 rA	61	Critical Low noise	~3ft	cylindrical
4	2	CCC Power Supply	CTI or Custom	3	AC power	15ft?	cylindrical

1.5.2 Rack#1 cabling Diagram



1.5.3 Temperature cable

The temperature cable is a 55 pin, straight through (except for shield connection), molded cable assembly manufactured by Glenair. See the Appendix for the cable spreadsheet.

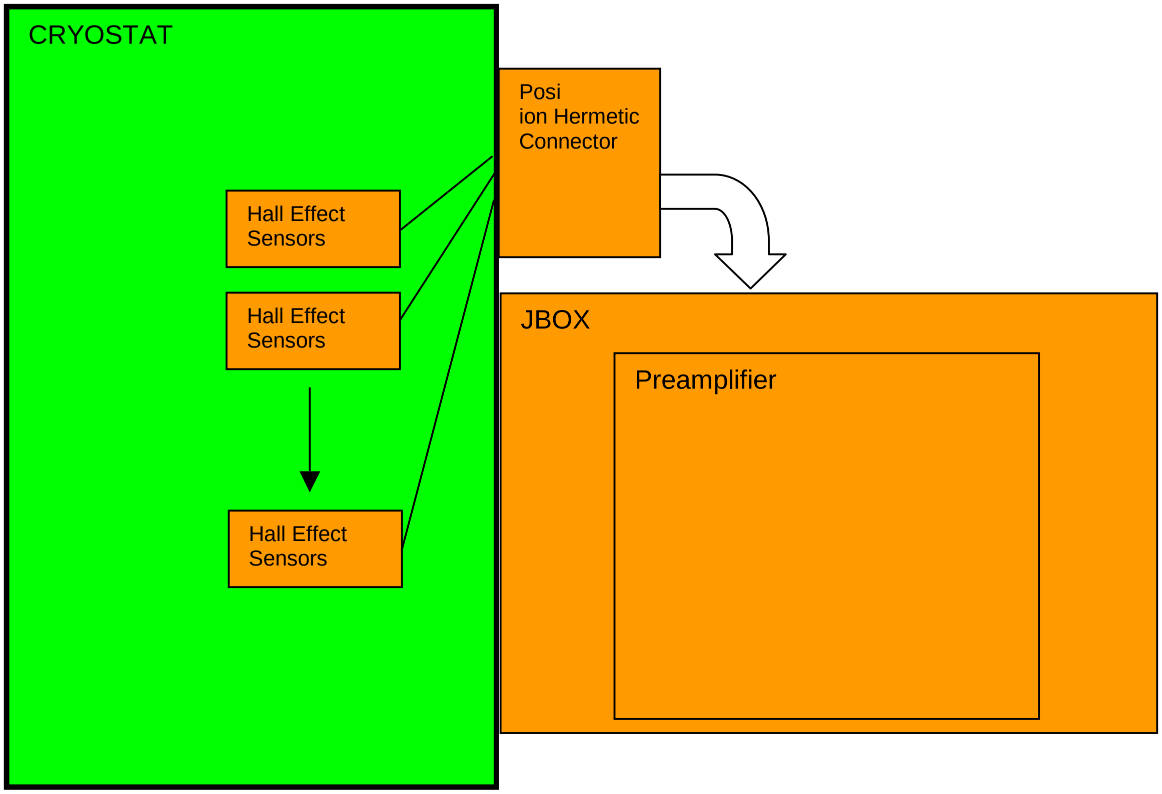
1.5.4 Motor cable

The motor cable is a 55 pin, straight through (except for shield connection), molded cable assembly manufactured by Glenair. See the Appendix for the cable spreadsheet.

1.5.5 JBOX

The Junction or JBOX provides the functions of:

1. Providing a convenient location to fanout the motor control and position signals to each motor.
2. Is the location for a magnetic Hall Effect sensor preamplifier.

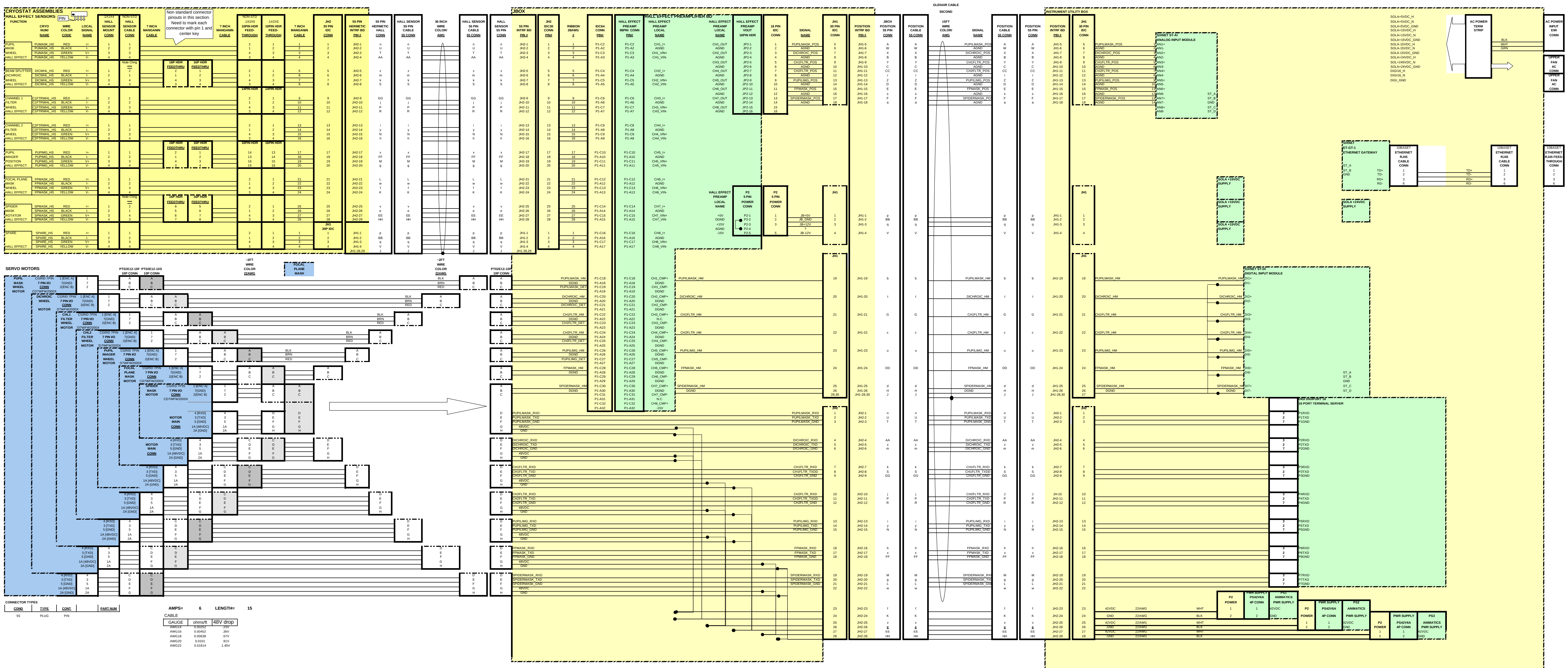


1.5.6 Array Cabling

Connection to the arrays are made via Glenair custom 61 pin cables specifically designed for low noise, high shielding operation. See the Appendix for the spreadsheet of array signal mapping and connections.

ALLADIN 2 pinout (SB0152 ROIC PCHANNEL OUTPUTS)					700-150			700-151					xxx					700-149					600-010				700-148					Backplane		
socket Yamaichi IC51-1244-410-1					Array Fanout			Config bd	J1,2,3,4= 2mm P1,2=96 pin				Thermal feedthrough		COLD	WARM		61 pin Bd	J1,2=34 pin headers				61 pin CABLES	conn=MS	conn=MS3116-E		60 pin Bd			J1,2=34 pin headers				
pin num	signal name	high level	low level		signal	conn	pin	signal	conn	pin	conn	pin	signal		pin	pin	Cu?	signal	conn	pin	pin	bd#	signal	cable#	pin	cond/shld	signal	pin	bd#	conn	pin	signal	slot#	pin
1	Q1_VGGCL	VDETCOM	-5	clk	q1_VGGCL	J1	1	VGGCL_T	J1	1	P1	A2,B2	VGGCL_T	JH1_T	4	3		VGGCL_T	J1	3	a	1	VGGCL_T	T-Q1&2	a	cond	VGGCL_T	a	1	J1	3	VGGCL_T	slot_7	C17
2	Q1_VDDCL	-1.2	VDDUC	clk	q1_VDDCL	J1	3	VDDCL_T	J1	3	P1	A27,B27	VDDCL_T	JH2_T	20	19		VDDCL_T	J2	19	LL	1	VDDCL_T	T-Q1&2	LL	shield	VDDCL_T	LL	1	J2	19	VDDCL_T	slot_1	C17
3	Q1_VDDUC	-4.0 to -3.5		bias	q1_VDDUC	J1	5	VDDUC_T	J1	5	P1	C27	VDDUC_T	JH2_T	19	20		VDDUC_T	J2	20	KK	1	VDDUC_T	T-Q1&2	KK	cond	VDDUC_T	KK	1	J2	20	VDDUC_T	slot_7	C28
4	Q1_PHISS	VpROW&COL	VnROW	clk	q1_PSS	J1	7	PSS_T	J1	7	P1	A28,B28	PSS_T	JH2_T	22	21		PSS_T	J2	21	AA	1	PSS_T	T-Q1&2	AA	shield	PSS_T	AA	1	J2	21	PSS_T	slot_7	C31
5	Q1_PHIS1	VpROW&COL	VnROW	clk	q1_PS1	J1	9	PS1_T	J1	9	P1	C28	PS1_T	JH2_T	22	21		PS1_T	J2	22	z	1	PS1_T	T-Q1&2	z	cond	PS1_T	z	1	J2	22	PS1_T	slot_1	C19
6	Q1_PHIS2	VpROW&COL	VnROW	clk	q1_PS2	J1	11	PS2_T	J1	11	P1	A29,B29	PS2_T	JH2_T	24	23		PS2_T	J2	23	i	1	PS2_T	T-Q1&2	i	shield	PS2_T	i	1	J2	23	PS2_T	slot_1	C21
7	Q1_PHIROE	VpROW&COL	VnROW	clk	q1_PROE	J1	13	PROE_T	J1	13	P1	C29	PROE_T	JH2_T	23	24		PROE_T	J2	24	h	1	PROE_T	T-Q1&2	h	cond	PROE_T	h	1	J2	24	PROE_T	slot_1	C23
8	Q1_PHIDES	VpROW&COL	VnROW	clk	q1_PDES	J1	15	PDES_T	J1	15	P1	A30,B30	PDES_T	JH2_T	26	25		PDES_T	J2	25	H	1	PDES_T	T-Q1&2	H	shield	PDES_T	H	1	J2	25	PDES_T	slot_1	C25
9	Q1_PHIFS	VpROW&COL	VnCOL	clk	q1_PFS	J1	17	PFS_T	J1	17	P1	C30	PFS_T	JH2_T	25	26		PFS_T	J2	26	G	1	PFS_T	T-Q1&2	G	cond	PFS_T	G	1	J2	26	PFS_T	slot_1	C27
10	Q1_PHIF1	VpROW&COL	VnCOL	clk	q1_PF1	J1	19	PF1_T	J1	19	P1	A31,B31	PF1_T	JH2_T	28	27		PF1_T	J2	27	K	1	PF1_T	T-Q1&2	K	shield	PF1_T	K	1	J2	27	PF1_T	slot_1	C29
11	Q1_PHIF2	VpROW&COL	VnCOL	clk	q1_PF2	J1	21	PF2_T	J1	21	P1	C31	PF2_T	JH2_T	27	28		PF2_T	J2	28	J	1	PF2_T	T-Q1&2	J	cond	PF2_T	J	1	J2	28	PF2_T	slot_1	C31
12	Q1_VnROW	-6.0 to -5.6		bias	q1_VNROW	J1	23	VNROW_T	J1	23	P1	A32,B32	VNROW_T	JH2_T	30	29		VNROW_T	J2	29	k	1	VNROW_T	T-Q1&2	k	shield	VNROW_T	k	1	J2	29	VNROW_T	slot_7	C30
13	Q1_VnCOL	-6.0 to -3.5		bias	q1_VNCOL	J1	25	VNCOL_T	J1	25	P1	C32	VNCOL_T	JH2_T	29	30		VNCOL_T	J2	30	j	1	VNCOL_T	T-Q1&2	j	cond	VNCOL_T	j	1	J2	30	VNCOL_T	slot_7	C29
14	Q1_Vp	0.0 to -0.5		bias	q1_VP	J1	27	VP_T	J1	27	P1	A1,B1	VP_T	JH1_T	2	1	Cu	VP_T	J1	1	Z	1	VP_T	T-Q1&2	Z	cond	VP_T	Z	1	J1	1	VP_T	AGND1	A12S?
15	VSS	0		bias	q1_VSSCM	J1	29	VSSCM_T	J1	29	P1	C2	VSSCM_T	JH1_T	3	4		VSSCM_T	J2	4	u	1	VSSCM_T	T-Q1&2	u	shield	VSSCM_T	u	1	J2	4	VSSCM_T	AGND7	A22s?
16	VSUB	0 gnd		bias	AGND	J1	31	AGND	J1	31	P1	C1	AGND_T	JH1_T	1	2	Cu	AGND_T	J1	2	Y	1	AGND_T	T-Q1&2	Y	shield	AGND_T	Y	1	J1	2	AGND_T	AGND2	A2s?
17	VSS	0		bias	q3_VSSCM	J1	33	VSSCM_B	J1	33	P2	C2	VSSCM_B	JH1_B	3	4		VSSCM_B	J1	4	u	2	VSSCM_B	B-Q3&4	u	shield	VSSCM_B	u	2	J1	4	VSSCM_B	AGND6	A12s?
18	Q3_Vp	0.0 to -0.5		bias	q3_VP	J1	35	VP_B	J1	35	P2	A1,B1	VP_B	JH1_B	1	2	Cu	VP_B	J1	2	Y	2	VP_B	B-Q3&4	Y	Y	VP_B	Y	2	J1	2	VP_B	AGND4	A2s?
19	Q3_VnCOL	-6.0 to -3.5		bias	q3_VNCOL	J1	37	VNCOL_B	J1	37	P2	C32	VNCOL_B	JH2_B	29	30		VNCOL_B	J2	30	j	2	VNCOL_B	B-Q3&4	j	cond	VNCOL_B	j	2	J2	30	VNCOL_B	slot_14	C29
20	Q3_VnROW	-6.0 to -5.6		bias	q3_VNROW	J1	39	VNROW_B	J1	39	P2	A32,B32	VNROW_B	JH2_B	30	29		VNROW_B	J2	29	k	2	VNROW_B	B-Q3&4	k	shield	VNROW_B	k	2	J2	29	VNROW_B	slot_14	C30
21	Q3_PHIF2	VpROW&COL	VnCOL	clk	q3_PF2	J1	41	PF2_B	J1	41	P2	C31	PF2_B	JH2_B	27	28		PF2_B	J2	28	J	2	PF2_B	B-Q3&4	J	cond	PF2_B	J	2	J2	28	PF2_B	slot_8	C31
22	Q3_PHIF1	VpROW&COL	VnCOL	clk	q3_PF1	J1	43	PF1_B	J1	43	P2	A31,B31	PF1_B	JH2_B	28	27		PF1_B	J2	27	K	2	PF1_B	B-Q3&4	K	shield	PF1_B	K	2	J2	27	PF1_B	slot_8	C29
23	Q3_PHIFS	VpROW&COL	VnCOL	clk	q3_PFS	J1	45	PFS_B	J1	45	P2	C30	PFS_B	JH2_B	25	26		PFS_B	J2	26	G	2	PFS_B	B-Q3&4	G	cond	PFS_B	G	2	J2	26	PFS_B	slot_8	C27
24	Q3_PHIDES	VpROW&COL	VnROW	clk	q3_PDES	J1	47	PDES_B	J1	47	P2	A30,B30	PDES_B	JH2_B	26	25		PDES_B	J2	25	H	2	PDES_B	B-Q3&4	H	shield	PDES_B	H	2	J2	25	PDES_B	slot_8	C25
25	Q3_PHIROE	VpROW&COL	VnROW	clk	q3_PROE	J1	49	PROE_B	J1	49	P2	C29	PROE_B	JH2_B	23	24		PROE_B	J2	24	h	2	PROE_B	B-Q3&4	h	cond	PROE_B	h	2	J2	24	PROE_B	slot_8	C23
26	Q3_PHIS2	VpROW&COL	VnROW	clk	q3_PS2	J1	51	PS2_B	J1	51	P2	A29,B29	PS2_B	JH2_B	24	23		PS2_B	J2	23	i	2	PS2_B	B-Q3&4	i	shield	PS2_B	i	2	J2	23	PS2_B	slot_8	C21
27	Q3_PHIS1	VpROW&COL	VnROW	clk	q3_PS1	J1	53	PS1_B	J1	53	P2	C28	PS1_B	JH2_B	21	22		PS1_B	J2	22	z	2	PS1_B	B-Q3&4	z	cond	PS1_B	z	2	J2	22	PS1_B	slot_8	C19
28	Q3_PHISS	VpROW&COL	VnROW	clk	q3_PSS	J1	55	PSS_B	J1	55	P2	A28,B28	PSS_B	JH2_B	22	21		PSS_B	J2	21	AA	2	PSS_B	B-Q3&4	AA	shield	PSS_B	AA	2	J2	21	PSS_B	slot_14	C31
29	Q3_VDDUC	-4.0 to -3.5		bias	q3_VDDUC	J1	57	VDDUC_B	J1	57	P2	C27	VDDUC_B	JH2_B	19	20		VDDUC_B	J2	20	KK	2	VDDUC_B	B-Q3&4	KK	cond	VDDUC_B	KK	2	J2	20	VDDUC_B	slot_14	C28
30	Q3_VDDCL	-1.2	VDDUC	clk	q3_VDDCL	J1	59	VDDCL_B	J1	59	P2	A27,B27	VDDCL_B	JH2_B	20	19		VDDCL_B	J2	19	LL	2	VDDCL_B	B-Q3&4	LL	shield	VDDCL_B	LL	2	J2	19	VDDCL_B	slot_8	C17
31	Q3_VGGCL	VDETCOM	-5	clk	q3_VGGCL	J1	60	VGGCL_B	J1	60	P2	A2,B2	VGGCL_B	JH1_B	4	3		VGGCL_B	J1	3	a	2	VGGCL_B	B-Q3&4	a	cond	VGGCL_B	a	2	J1	3	VGGCL_B	slot_14	C17
32	Q3_TEND				q3_TEND	J2	1	Q3_TEND	J2	1	P2	C15	Q3_TEND	JH1_B	29	30		Q3_TEND	J1	30	nc	2					Q3_TEND	nc	2	J1	30	Q3_TEND		
33	Q3_VRSTG	-3.5	-5.6	clk	q3_VRSTG	J2	3	VRSTG_B	J2	3	P2	C3	VRSTG_B	JH1_B	5	6		VRSTG_B	J1	6	FF	2	VRSTG_B	B-Q3&4	FF	cond	VRSTG_B	FF	2	J1	6	VRSTG_B	slot_14	C23
34	Q3_VROWOFF	0.0 to -0.7			q3_VROWOFF	J2	5	VROWOFF_B	J2	5	P2	A4,B4	VROWOFF_B	JH1_B	8	7		VROWOFF_B	J1	7	t	2	VROWOFF_B	B-Q3&4	t	shield	VROWOFF_B	t	2	J1	7	VROWOFF_B	AGND5	A22s?
35	Q3_IREF	-1.5 to -2.5		Isource	q3_IREF	J2	7	VIREF_B	J2	7	P2	C4	VIREF_B	JH1_B	7	8		VIREF_B	J1	8	s	2	VIREF_B	B-Q3&4	s	cond	VIREF_B	s	2	J1	8	VIREF_B	slot_14	C25
36	Q3_VROWON	-6.0 to -5.6			q3_VROWON	J2	9	VROWON_B	J2	9	P2	A3,B3	VROWON_B	JH1_B	6	5		VROWON_B	J1	5	GG	2	VROWON_B	B-Q3&4	GG	shield	VROWON_B	GG	2	J1	5	VROWON_B	slot_14	C19
37	Q3_VRSTR	-3.5	-5.6	clk	q3_VRSTR	J2	11	VRSTR_B	J2	11	P2	A5,B5	VRSTR_B	JH1_B	10	9		VRSTR_B	J1	9	MM	2	VRSTR_B	B-Q3&4	MM	cond	VRSTR_B	MM	2	J1	9	VRSTR_B	slot_14	C21
38	Q3_OUT1			output	q3_OUT1	J2	13	Q3OUT1+	J2	13	P2	C6	Q3OUT1+	JH1_B	11	12		Q3OUT1+	J1	12	DD	2	Q3OUT1+	B-Q3&4	DD	cond	Q3OUT1+	DD	2	J1	12	Q3OUT1+	slot_13	C3
39	Q3_OUT2			output	q3_OUT2	J2	15	Q3OUT2+	J2	15	P2	C7	Q3OUT2+	JH1_B	13	14		Q3OUT2+	J1	14	W	2	Q3OUT2+	B-Q3&4	W	cond	Q3OUT2+	W	2	J1	14	Q3OUT2+	slot_13	C5
40	Q3_OUT3			output	q3_OUT3	J2	17	Q3OUT3+	J2	17	P2	C8	Q3OUT3+	JH1_B	15	16		Q3OUT3+	J1	16	g	2	Q3OUT3+	B-Q3&4	g	cond	Q3OUT3+	g	2	J1	16	Q3OUT3+	slot_13	C7
41	Q3_OUT4			output	q3_OUT4	J2	19	Q3OUT4+	J2	19	P2	C9	Q3OUT4+	JH1_B	17	18		Q3OUT4+	J1	18	U	2	Q3OUT4+	B-Q3&4	U	cond	Q3OUT4+	U	2	J1	18	Q3OUT4+	slot_13	C9
42	Q3_OUT5			output	q3_OUT5	J2	21	Q3OUT5+	J2	21	P2	C10	Q3OUT5+	JH1_B	19	20		Q3OUT5+	J1	20	S	2	Q3OUT5+	B-Q3&4	S	cond	Q3OUT5+	S	2	J1	20	Q3OUT5+	slot_13	C11
43	Q3_OUT6			output	q3_OUT6	J2	23	Q3OUT6+	J2	23	P2	C11	Q3OUT6+	JH1_B	21	22		Q3OUT6+	J1	22	n	2	Q3OUT6+	B-Q3&4	n	cond	Q3OUT6+	n	2	J1	22	Q3OUT6+	slot_13	C13
44	Q3_OUT7			output	q3_OUT7	J2	25	Q3OUT7+	J2	25	P2	C12	Q3OUT7+	JH1_B	23	24		Q3OUT7+	J1	24	BB	2	Q3OUT7+	B-Q3&4	BB	cond	Q3OUT7+	BB	2	J1	24	Q3OUT7+	slot_13	C15
45	Q3_OUT8			output	q3_OUT8	J2	27	Q3OUT8+	J2	27	P2	C13	Q3OUT8+	JH1_B	25	26		Q3OUT8+	J1	26	P	2	Q3OUT8+	B-Q3&4	P	cond	Q3OUT8+	P	2	J1	26	Q3OUT8+	slot_13	C17
46	Q3_VDDOUT	-1.0 to -1.3		bias	q3_VDDOUT	J2	29	VDDOUT_B	J2	29	P2	C14	VDDOUT_B	JH1&2	27_1	28_2	_Cu	VDDOUT_B	J1&2	28_2	N_A	2	VDDOUT_B	B-Q3&4	N_A	c_s	VDDOUT_B	N_A	2	J1&2	28_2	VDDOUT_B	slot_14	C26
47	Q3_VDETCOM	-2.8 to-3.4		bias	q3_VDETCOM	J2	31	VDETCOM	J2	31	P2	A18,B18	VDETCOM_B	JH2_B	2	1	Cu	VDETCOM_B	J2	1	B	2	VDETCOM_B	B-Q3&4	B	cond	VDETCOM_B	B	2	J2	1	VDETCOM_B	slot_14	C27
48	Q4_VDDOUT	-1.0 to -1.3		bias	q3_VDDOUT	J2	33	VDDOUT_B	J2	33	P2	*	*	*	*	*		*	*	*	*	*	*	B-Q3&4	*	*	*	*	*	*	*	*		
49	Q4_OUT8			output	q4_OUT8	J2	35	Q4OUT8+	J2	35	P2	C19	Q4OUT8+	JH2_B	3	4		Q4OUT8+	J2	4	b	2	Q4OUT8+	B-Q3&4	b	cond	Q4OUT8+	b	2	J2	4	Q4OUT8+	slot_10	C17
50	Q4_OUT7			output	q4_OUT7	J2	37	Q4OUT7+	J2	37	P2	C20	Q4OUT7+	JH2_B	5	6		Q4OUT7+	J2	6	v		Q4OUT7+	B-Q3&4	v	cond	Q4OUT7+	v		J2	6	Q4OUT7+	slot_10	C15
51	Q4_OUT6			output	q4_OUT6	J2	39	Q4OUT6+	J2	39	P2	C21	Q4OUT6+	JH2_B	7	8		Q4OUT6+	J2	8	d		Q4OUT6+	B-Q3&4	d	cond	Q4OUT6+	d		J2	8	Q4OUT6+	slot_10	C13
52	Q4_OUT5			output	q4_OUT5	J2	41	Q4OUT5+	J2	41	P2	C22	Q4OUT5+	JH2_B	9	10		Q4OUT5+	J2	10	HH		Q4OUT5+	B-Q3&4	HH	cond	Q4OUT5+	HH		J2	10	Q4OUT5+	slot_10	C11
53	Q4_OUT4			output	q4_OUT4	J2	43	Q4OUT4+	J2	43	P2	C23	Q4OUT4+	JH2_B	11	12		Q4OUT4+	J2	12	x		Q4OUT4+	B-Q3&4	x	cond	Q4OUT4+	x		J2	12	Q4OUT4+	slot_10	C9
54	Q4_OUT3			output	q4_OUT3	J2	45	Q4OUT3+	J2	45	P2	C24	Q4OUT3+	JH2_B	13	14		Q4OUT3+	J2	14	C		Q4OUT3+	B-Q3&4	C	cond	Q4OUT3+	C		J2	13	Q4OUT3+	slot_10	C7
55	Q4_OUT2			output	q4_OUT2	J2	47	Q4OUT2+	J2	47	P2	C25	Q4OUT2+	JH2_B	15	16		Q4OUT2+	J2	16	f		Q4OUT2+	B-Q3&4	f	cond	Q4OUT2+	f		J2	16	Q4OUT2+	slot_10	C5
56	Q4_OUT1			output	q4_OUT1	J2	49	Q4OUT1+	J2	49	P2	C26	Q4OUT1+	JH2_B	17	18		Q4OUT1+	J2	18	E		Q4OUT1+	B-Q3&4	E	cond	Q4OUT1+	E		J2	18	Q4OUT1+	slot_10	C3
57	Q4_VRSTR	-3.5	-5.6	clk	q4_VRSTR	J2	51	VRSTR_B	J2	51	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
58	Q4_VROWON	-6.0 to -5.6			q4_VROWON	J2	53	VROWON_B	J2	53	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
59	Q4_IREF	-1.5 to -2.5		Isource	q4_IREF	J2	55	VIREF_B	J2	55	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
60	Q4_VROWOFF	0.0 to -0.7			q4_VROWOFF	J2	57	VROWOFF_B	J2	57	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
61	Q4_VRSTG	-3.5	-5.6	clk	q4_VRSTG	J2	59	VRSTG_B	J2	59	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
62	Q4_TEND				q4_TEND	J2	60	Q4_TEND	J2	60	P2	C17	Q4_TEND	JH2_B	33	34		Q4_TEND	J2	34	NC						Q4_TEND	NC		J2	34	Q4_TEND		
63	Q4_VGGCL	VDETCOM	-5	clk	q4_VGGCL	J3	1	VGGCL_B	J3	1	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
64	Q4_VDDCL	-1.2	VDDUC	clk	q4_VDDCL	J3	3	VDDCL_B	J3	3	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
65	Q4_VDDUC	-4.0 to -3.5		bias	Q4_VDDUC	J3	5	VDDUC_B	J3	5	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
66	Q4_PHISS	VpROW&COL	VnROW	clk	q4_PSS	J3	7	PSS_B	J3	7	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
67	Q4_PHIS1	VpROW&COL	VnROW	clk	q4_PS1	J3	9	PS1_B	J3	9	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
68	Q4_PHIS2	VpROW&COL	VnROW	clk	q4_PS2	J3	11	PS2_B	J3	11	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
69	Q4_PHIROE	VpROW&COL	VnROW	clk	q4_PROE	J3	13	PROE_B	J3	13	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
70	Q4_PHIDES	VpROW&COL	VnROW	clk	q4_PDES	J3	15	PDES_B	J3	15	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
71	Q4_PHIFS	VpROW&COL	VnCOL	clk	q4_PFS	J3	17	PFS_B	J3	17	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
72	Q4_PHIF1	VpROW&COL	VnCOL	clk	q4_PF1	J3	19	PF1_B	J3	19	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
73	Q4_PHIF2	VpROW&COL	VnCOL	clk	q4_PF2	J3	21	PF2_B	J3	21	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
74	Q4_VnROW	-6.0 to -5.6		bias	q4_VNROW	J3	23	VNROW_B	J3	23	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
75	Q4_VnCOL	-6.0 to -3.5		bias	q4_VNCOL	J3	25	VNCOL_B	J3	25	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
76	Q4_VP	0.0 to -0.5		bias	q4_VP	J3	27	VP_B	J3	27	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
77	VSS	0		bias	q4_VSSCM	J3	29	VSSCM_B	J3	29	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
78	VSUB	0 gnd		bias	AGND	J3	31	AGND	J3	31	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
79	VSS	0		bias	q2_VSSCM	J3	33	VSSCM_T	J3	33	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
80	Q2_Vp	0.0 to -0.5		bias	q2_VP	J3	35	VP_T	J3	35	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
81	Q2_VnCOL	-6.0 to -3.5		bias	q2_VNCOL	J3	37	VNCOL_T	J3	37	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
82	Q2_VnROW	-6.0 to -5.6		bias	q2_VNROW	J3	39	VNROW_T	J3	39	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
83	Q2_PHIF2	VpROW&COL	VnCOL	clk	q2_PF2	J3	41	PF2_T	J3	41	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
84	Q2_PHIF1	VpROW&COL	VnCOL	clk	q2_PF1	J3	43	PF1_T	J3	43	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
85	Q2_PHIFS	VpROW&COL	VnCOL	clk	q2_PFS	J3	45	PFS_T	J3	45	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
86	Q2_PHIDES	VpROW&COL	VnROW	clk	q2_PDES	J3	47	PDES_T	J3	47	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
87	Q2_PHIROE	VpROW&COL	VnROW	clk	q2_PROE	J3	49	PROE_T	J3	49	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
88	Q2_PHIS2	VpROW&COL	VnROW	clk	q2_PHIS2	J3	51	PS2_T	J3	51	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
89	Q2_PHIS1	VpROW&COL	VnROW	clk	q2_PS1	J3	53	PS1_T	J3	53	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		

90	Q2_PHISS	VpROW&COL	VnROW	clk	q2_PSS	J3	55	PSS_T	J3	55	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
91	Q2_VDDUC	-4.0 to -3.5		bias	q2_VDDUC	J3	57	VDDUC_T	J3	57	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
92	Q2_VDDCL	-1.2	VDDUC	clk	q2_VDDCL	J3	59	VDDCL_T	J3	59	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
93	Q2_VGGCL	VDETCOM	-5	clk	q2_VGGCL	J3	60	VDDCL_T	J3	60	P2	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
94	Q2_TEND				q2_TEND	J4	1	Q2TEND	J4	1	P1	C17	Q2TEND	JH1_T	33	34		Q2TEND									Q2TEND					Q2TEND		
95	Q2_VRSTG	-3.5	-5.6	clk	q2_VRSTG	J4	3	VRSTG_T	J4	3	P1	C3	VRSTG_T	JH1_T	5	6		VRSTG_T	J1	6	FF	1	VRSTG_T	T-Q1&2	FF	cond	VRSTG_T	FF	1	J1	6	VRSTG_T	slot_7	C23
96	Q2_VROWOFF	0.0 to -0.7			q2_VROWOFF	J4	5	VROWOFF_T	J4	5	P1	A4,B4	VROWOFF_T	JH1_T	5	5		VROWOFF_T	J1	5	t	1	VROWOFF_T	T-Q1&2	t	shield	VROWOFF_T	t	1	J1	5	VROWOFF_T	AGND3	
97	Q2_IREF	-1.5 to -2.5		Isource	q2_IREF	J4	7	VIREF_T	J4	7	P1	C4	VIREF_T	JH1_T	7	8		VIREF_T	J1	8	s	1	VIREF_T	T-Q1&2	s	cond	VIREF_T	s	1	J1	8	VIREF_T	slot_7	C25
98	Q2_VROWON	-6.0 to -5.6			q2_VROWON	J4	9	VROWON_T	J4	9	P1	A3,B3	VROWON_T	JH1_T	8	7		VROWON_T	J1	7	GG	1	VROWON_T	T-Q1&2	GG	shield	VROWON_T	GG	1	J1	7	VROWON_T	slot_7	C19
99	Q2_VRSTR	-3.5	-5.6	clk	q2_VRSTR	J4	11	VRSTR_T	J4	11	P1	A5,B5	VRSTR_T	JH1_T	10	9		VRSTR_T	J1	9	MM	1	VRSTR_T	T-Q1&2	MM	shield	VRSTR_T	MM	1	J1	9	VRSTR_T	slot_7	C21
100	Q2_OUT1			output	q2_OUT1	J4	13	Q2OUT1+	J4	13	P1	C26	Q2OUT1+	JH2_T	17	18		Q2OUT1+	J2	18	E	1	Q2OUT1+	T-Q1&2	E	cond	Q2OUT1+	E	1	J2	18	Q2OUT1+	slot_3	C3
101	Q2_OUT2			output	q2_OUT2	J4	15	Q2OUT2+	J4	15	P1	C25	Q2OUT2+	JH2_T	15	16		Q2OUT2+	J2	16	f	1	Q2OUT2+	T-Q1&2	f	cond	Q2OUT2+	f	1	J2	16	Q2OUT2+	slot_3	C5
102	Q2_OUT3			output	q2_OUT3	J4	17	Q2OUT3+	J4	17	P1	C24	Q2OUT3+	JH2_T	13	14		Q2OUT3+	J2	14	C	1	Q2OUT3+	T-Q1&2	C	cond	Q2OUT3+	C	1	J2	14	Q2OUT3+	slot_3	C7
103	Q2_OUT4			output	q2_OUT4	J4	19	Q2OUT4+	J4	19	P1	C23	Q2OUT4+	JH2_T	11	12		Q2OUT4+	J2	12	x	1	Q2OUT4+	T-Q1&2	x	cond	Q2OUT4+	x	1	J2	12	Q2OUT4+	slot_3	C9
104	Q2_OUT5			output	q2_OUT5	J4	21	Q2OUT5+	J4	21	P1	C22	Q2OUT5+	JH2_T	9	10		Q2OUT5+	J2	10	HH	1	Q2OUT5+	T-Q1&2	HH	cond	Q2OUT5+	HH	1	J2	10	Q2OUT5+	slot_3	C11
105	Q2_OUT6			output	q2_OUT6	J4	23	Q2OUT6+	J4	23	P1	C21	Q2OUT6+	JH2_T	7	8		Q2OUT6+	J2	8	d	1	Q2OUT6+	T-Q1&2	d	cond	Q2OUT6+	d	1	J2	8	Q2OUT6+	slot_3	C13
106	Q2_OUT7			output	q2_OUT7	J4	25	Q2OUT7+	J4	25	P1	C20	Q2OUT7+	JH2_T	5	6		Q2OUT7+	J2	6	v	1	Q2OUT7+	T-Q1&2	v	cond	Q2OUT7+	v	1	J2	6	Q2OUT7+	slot_3	C15
107	Q2_OUT8			output	q2_OUT8	J4	27	Q2OUT8+	J4	27	P1	C19	Q2OUT8+	JH2_T	3	4		Q2OUT8+	J2	4	b	1	Q2OUT8+	T-Q1&2	b	cond	Q2OUT8+	b	1	J2	4	Q2OUT8+	slot_3	C17
108	Q2_VDDOUT	-1.0 to -1.3		bias	q2_VDDOUT	J4	29	VDDOUT_T	J4	29	P1	C14,?C18	VDDOUT_T	JH1&2	27_1	28_2	_Cu	VDDOUT_T	J1&2	28_2	N_A	1	VDDOUT_T	T-Q1&2	N_A	c_s	VDDOUT_T	N_A	1	J1&2	28_2	VDDOUT_T	slot_7	C26
109	VDETCOM	-2.8 to-3.4		bias	VDETCOM	J4	31	VDETCOM	J4	31	P1	A18,B18	VDETCOM	JH2_T	2	1	Cu	VDETCOM	J2	1	B	1	VDETCOM	T-Q1&2	B	cond	VDETCOM	B	1	J2	1	VDETCOM	slot_7	C27
110	Q1_VDDOUT	-1.0 to -1.3		bias	q1_VDDOUT	J4	33	VDDOUT_T	J4	33	P1	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
111	Q1_OUT8			output	q1_OUT8	J4	35	Q1OUT8+	J4	35	P1	C13	Q1OUT8+	JH1_T	25	26		Q1OUT8+	J1	26	P	1	Q1OUT8+	T-Q1&2	P	cond	Q1OUT8+	P	1	J1	26	Q1OUT8+	slot_6	C17
112	Q1_OUT7			output	q1_OUT7	J4	37	Q1OUT7+	J4	37	P1	C12	Q1OUT7+	JH1_T	23	24		Q1OUT7+	J1	24	BB	1	Q1OUT7+	T-Q1&2	BB	cond	Q1OUT7+	BB	1	J1	24	Q1OUT7+	slot_6	C15
113	Q1_OUT6			output	q1_OUT6	J4	39	Q1OUT6+	J4	39	P1	C11	Q1OUT6+	JH1_T	21	22		Q1OUT6+	J1	22	n	1	Q1OUT6+	T-Q1&2	n	cond	Q1OUT6+	n	1	J1	22	Q1OUT6+	slot_6	C13
114	Q1_OUT5			output	q1_OUT5	J4	41	Q1OUT5+	J4	41	P1	C10	Q1OUT5+	JH1_T	19	20		Q1OUT5+	J1	20	S	1	Q1OUT5+	T-Q1&2	S	cond	Q1OUT5+	S	1	J1	20	Q1OUT5+	slot_6	C11
115	Q1_OUT4			output	q1_OUT4	J4	43	Q1OUT4+	J4	43	P1	C9	Q1OUT4+	JH1_T	17	18		Q1OUT4+	J1	18	U	1	Q1OUT4+	T-Q1&2	U	cond	Q1OUT4+	U	1	J1	18	Q1OUT4+	slot_6	C9
116	Q1_OUT3			output	q1_OUT3	J4	45	Q1OUT3+	J4	45	P1	C8	Q1OUT3+	JH1_T	15	16		Q1OUT3+	J1	16	g	1	Q1OUT3+	T-Q1&2	g	cond	Q1OUT3+	g	1	J1	16	Q1OUT3+	slot_6	C7
117	Q1_OUT2			output	q1_OUT2	J4	47	Q1OUT2+	J4	47	P1	C7	Q1OUT2+	JH1_T	13	14		Q1OUT2+	J1	14	W	1	Q1OUT2+	T-Q1&2	W	cond	Q1OUT2+	W	1	J1	14	Q1OUT2+	slot_6	C5
118	Q1_OUT1			output	q1_OUT1	J4	49	Q1OUT1+	J4	49	P1	C6	Q1OUT1+	JH1_T	11	12		Q1OUT1+	J1	12	DD	1	Q1OUT1+	T-Q1&2	DD	cond	Q1OUT1+	DD	1	J1	12	Q1OUT1+	slot_6	C3
119	Q1_VRSTR	-3.5	-5.6	clk	q1_VRSTR	J4	51	VRSTR_T	J4	51	P1	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
120	Q1_VROWON	-6.0 to -5.6			q1_VROWON	J4	53	VROWON_T	J4	53	P1	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
121	Q1_IREF	-1.5 to -2.5		Isource	q1_IREF	J4	55	VIREF_T	J4	55	P1	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
122	Q1_VROWOFF	0.0 to -0.7			q1_VROWOFF	J4	57	VROWOFF_T	J4	57	P1	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
123	Q1_VRSTG	-3.5	-5.6	clk	q1_VRSTG	J4	59	VRSTG_T	J4	59	P1	*	*	*	*	*		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*		
124	Q1_TEND				q1_TEND	J4	60	Q1TEND	J4	60	P1	C15	Q1TEND	JH1_T	30	29		Q1TEND	J1	29	PP	1	Q1TEND	T-Q1&2	PP	PP	Q1TEND	PP	1	J1	29	Q1TEND		


CRYOSTAT ASSEMBLIES
HALL EFFECT SENSORS
SERVO MOTORS
JBOX
INSTRUMENT UTILITY BOX
CONNECTOR TYPES
AMPS= 6 LENGTH= 15

TEMPERATURE CONTROL SUBSYSTEM

TEMPERATURE SENSORS AND HEATERS

FUNCTION LAKESHORE DT471-BR	CRYO NUM/ NAME	WIRE COLOR CODE	LOCAL SIGNAL NAME	.1X1X10 TEMP 10PIN CGRID CONN	.1X1X10 TEMP 10CON CGRID CONN	? INCH MANGANIN CABLE	NON-STD .1X2X5 16PIN HDR FEED-	.1X2X5 16PIN CON FEED-	? INCH MANGANIN	.1X1X8 8PIN CGRID	.1X1X8 8CON CGRID	? INCH MANGANIN	JH1 30 PIN IDC	55 PIN HERMETIC INTRF BD
RED	RED_I+	BLK/BLU	I+	3	3		1	2		1	1	1	1	JH1-1
ARRAY	RED_V+	YEL/CLR	V+	4	4		2	1		2	2	2	2	JH1-2
TEMP	RED_I-	RED	I-	5	5		3	4		3	3	3	3	JH1-3
SENSOR	RED_V-	GRN	V-	6	6		4	3		4	4	4	4	JH1-4
RED	RED+HTR1		R3||R4+	7	7		5	6		5	5	5	5	JH1-5
ARRAY	RED_HTR2		R3||R4-	8	8		6	5		6	6	6	6	JH1-6
HEATER	RED_HTR3		R1||R2+	9	9		7	8		7	7	7	7	JH1-7
RESISTORS	RED_HTR4		R1||R2-	10	10		8	7		8	8	8	8	JH1-8
				10PIN CGRID	10PIN CGRID		16PIN FD THRU	16 PIN FD THRU						
BLUE	BLU_I+	BLK/BLU	I+	3	3		1	2		1	1	9	9	JH1-9
ARRAY	BLU_V+	YEL/CLR	V+	4	4		2	1		2	2	10	10	JH1-10
TEMP	BLU_I-	RED	I-	5	5		3	4		3	3	11	11	JH1-11
SENSOR	BLU_V-	GRN	V-	6	6		4	3		4	4	12	12	JH1-12
BLUE	GUID_HTR		R3||R4+	7	7		5	6		5	5	13	13	JH1-13
ARRAY	GUID_HTR		R3||R4-	8	8		6	5		6	6	14	14	JH1-14
HEATER	GUID_HTR		R1||R2+	9	9		7	8		7	7	15	15	JH1-15
RESISTORS	GUID_HTR		R1||R2-	10	10		8	7		8	8	16	16	JH1-16
				4PIN CGRID	4PIN CGRID									
	STG1_TMP	BLK/BLU	I+	1	1							17	17	JH1-17
CCC 1ST STG	STG1_TMP	YEL/CLR	V+	2	2							18	18	JH1-18
TEMP	STG1_TMP	RED	I-	3	3							19	19	JH1-19
SENSOR	STG1_TMP	GRN	V-	4	4							20	20	JH1-20
				4PIN CGRID	4PIN CGRID									
	STG2_TMP	BLK/BLU	I+	1	1							21	21	JH1-21
CCC 2ND STG	STG2_TMP	YEL/CLR	V+	2	2							22	22	JH1-22
TEMP	STG2_TMP	RED	I-	3	3							23	23	JH1-23
SENSOR	STG2_TMP	GRN	V-	4	4							24	24	JH1-24
				4PIN CGRID	4PIN CGRID								JH2 30COND	
	CLDST_TMP	BLK/BLU	I+	1	1							17	1	JH2-1
COLD STRUCT	CLDST_TMP	YEL/CLR	V+	2	2							18	2	JH2-2
TEMP	CLDST_TMP	RED	I-	3	3							19	3	JH2-3
SENSOR	CLDST_TMP	GRN	V-	4	4							20	4	JH2-4
				4PIN CGRID	4PIN CGRID									
	RSHLD_TMP	BLK/BLU	I+	1	1							21	5	JH2-5
RAD SHLD	RSHLD_TMP	YEL/CLR	V+	2	2							22	6	JH2-6
TEMP	RSHLD_TMP	RED	I-	3	3							23	7	JH2-7
SENSOR	RSHLD_TMP	GRN	V-	4	4							24	8	JH2-8
				4PIN CGRID	4PIN CGRID									
	RSCCC_TMP	BLK/BLU	I+	1	1							17	9	JH2-9
RAD CCC 1ST	RSCCC_TMP	YEL/CLR	V+	2	2							18	10	JH2-10
TEMP	RSCCC_TMP	RED	I-	3	3							19	11	JH2-11
SENSOR	RSCCC_TMP	GRN	V-	4	4							20	12	JH2-12
														JH1-28,29
				4PIN CGRID	4PIN CGRID									
	RSHLD_TMP	BLK/BLU	I+	1	1							21	13	JH2-13
APD	RSHLD_TMP	YEL/CLR	V+	2	2							22	14	JH2-14
TEMP	RSHLD_TMP	RED	I-	3	3							23	15	JH2-15
SENSOR	RSHLD_TMP	GRN	V-	4	4							24	16	JH2-16

55 PIN HERMETIC INTRF BD	55 PIN HERMETIC TEMP	TEMP 55 PIN CABLE	GLENAIR 55COND CABLE / GLENAIR 55COND	TEMP 55 PIN CABLE	TEMP 55 PIN	55 PIN INTRF BD	SIGNAL	FILTER	DIN6-REAR PNL
									RED LAKESHORE MODEL 331 SENSOR CONN
JH1-1	p	p	RED_I+	p	p	JH1-1	RED_I+		5 [I+] CHNL A
JH1-2	BB	BB	RED_V+	BB	BB	JH1-2	RED_V+		4 [V+] CHNL A
JH1-3	q	q	RED_I-	q	q	JH1-3	RED_I-		1 [I-] CHNL A
JH1-4	V	V	RED_V-	V	V	JH1-4	RED_V-		2 [V-] CHNL A
									CK05 .1uF Cer Cap
JH1-5	A	A	RED_HTR1	A	A	JH1-5	RED_HTR1	HI	HI
JH1-6	W	W	RED_HTR2	W	W	JH1-6	RED_HTR2		
JH1-7	X	X	RED_HTR3	X	X	JH1-7	RED_HTR3	LO	LO
JH1-8	B	B	RED_HTR4	B	B	JH1-8	RED_HTR4	GND	GND
									BLUE MODEL 331
JH1-9	Y	Y	BLU_I+	Y	Y	JH1-9	BLU_I+		5 [I+] CHNL A
JH1-10	C	C	BLU_V+	C	C	JH1-10	BLU_V+		4 [V+] CHNL A
JH1-11	CC	CC	BLU_I-	CC	CC	JH1-11	BLU_I-		1 [I-] CHNL A
JH1-12	r	r	BLU_V-	r	r	JH1-12	BLU_V-		2 [V-] CHNL A
									CK05 .1uF BLUE
JH1-13	Z	Z	BLU_HTR1	Z	Z	JH1-13	BLU_HTR1	HI	HI
JH1-14	D	D	BLU_HTR2	D	D	JH1-14	BLU_HTR2		
JH1-15	E	E	BLU_HTR3	E	E	JH1-15	BLU_HTR3	LO	LO
JH1-16	s	s	BLU_HTR4	s	s	JH1-16	BLU_HTR4	GND	GND
									MONITOR MODEL218
JH1-17	F	F	STG1_I+	F	F	JH1-17	STG1_I+		IN1I+
JH1-18	a	a	STG1_V+	a	a	JH1-18	STG1_V+		IN1V+
JH1-19	b	b	STG1_I-	b	b	JH1-19	STG1_I-		IN1I-
JH1-20	t	t	STG1_V-	t	t	JH1-20	STG1_V-		IN1V-
JH1-21	G	G	STG2_I+	G	G	JH1-21	STG2_I+		IN2I+
JH1-22	c	c	STG2_V+	c	c	JH1-22	STG2_V+		IN2V+
JH1-23	u	u	STG2_I-	u	u	JH1-23	STG2_I-		IN2I-
JH1-24	DD	DD	STG2_V-	DD	DD	JH1-24	STG2_V-		IN2V-
JH2-1	n	n	STG2_I+	n	n	JH2-1	STG2_I+		IN3I+
JH2-2	U	U	STG2_V+	U	U	JH2-2	STG2_V+		IN3V+
JH2-3	T	T	STG2_I-	T	T	JH2-3	STG2_I-		IN3I-
JH2-4	AA	AA	STG2_V-	AA	AA	JH2-4	STG2_V-		IN3V-
JH2-5	z	z	STG2_I+	z	z	JH2-5	STG2_I+		IN4I+
JH2-6	m	m	STG2_V+	m	m	JH2-6	STG2_V+		IN4V+
JH2-7	k	k	STG2_I-	k	k	JH2-7	STG2_I-		IN4I-
JH2-8	S	S	STG2_V-	S	S	JH2-8	STG2_V-		IN4V-
JH2-9	GG	GG	STG2_I+	GG	GG	JH2-9	STG2_I+		IN5I+
JH2-10	j	j	STG2_V+	j	j	JH2-10	STG2_V+		IN5V+
JH2-11	P	P	STG2_I-	P	P	JH2-11	STG2_I-		IN5I-
JH2-12	R	R	STG2_V-	R	R	JH2-12	STG2_V-		IN5V-
JH1-28,29	J	J		J	J	JH1-28,29			
JH2-13	i	i	STG2_I+	i	i	JH2-13	STG2_I+		IN6I+
JH2-14	y	y	STG2_V+	y	y	JH2-14	STG2_V+		IN26+
JH2-15	N	N	STG2_I-	N	N	JH2-15	STG2_I-		IN6I-
JH2-16	h	h	STG2_V-	h	h	JH2-16	STG2_V-		IN6V-