

MONSOON Status

Barry Michael Starr

MONSOON Current Status

- System design has been in process since 12/00.
- Software design has been in process since spring of '01
- Key hardware technologies known
 - Id'd & prototyped at component level.
- Key software technologies id'd & evaluated
- 12 channel CCD prototype board (single board controller)
 - Qty 2 fabricated, in test
- Prototype master control board
 - Qty 2 fabricated, in test
- Prototype 36 channel IR acquisition board
 - In PCB fabrication

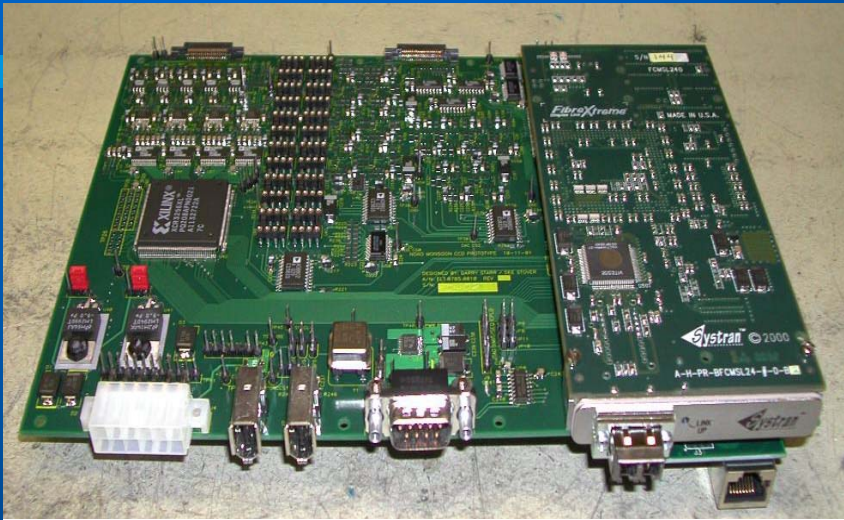
MONSOON CCD Prototype

- 12-channel 16-bit > 1 MHz acquisition
 - Preamp / CDS / ADC, 1/2/4/8/16 sample digital averaging
- 12-channel Hi-voltage low-noise bias
 - +/-40V range, 12-bit resolution, analog readback
- 12-channel Lo-voltage low-noise bias
 - +/-12V range, 12-bit resolution, analog readback
- 24-channel clock driver
 - +/-12V range, 12-bit resolution, analog readback
- CPLD clock pattern generator
- 50 Mpixel/sec bi-directional fiberlink
 - 1Gb/s fiber upgradeable to 2.4 Gb/s
- 20 MHz embedded processor
 - 10 Mb/s Ethernet link, TCP-IP stack
- Single board 6U Eurocard (VME) form factor

CCD Prototype Goals

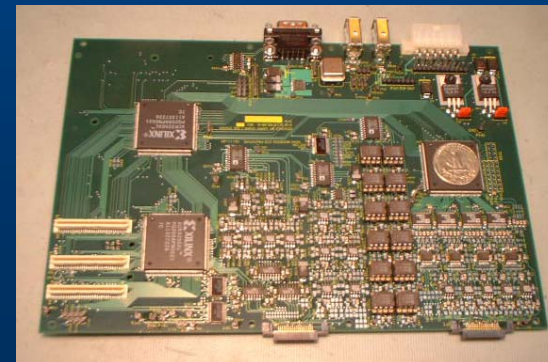
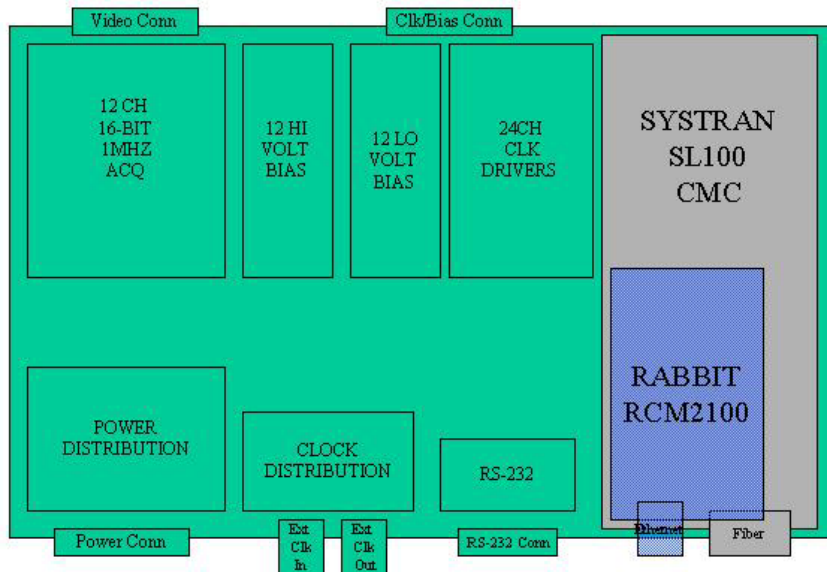
- Further Evaluate:
 - Key technologies
 - SL100 fiber
 - Rabbit RCM2100 embedded
 - AD9826 AFE
 - Op-amps
 - CCD Clock Drivers
 - CPLDs
 - Component packaging densities
 - Power consumption issues
 - Controller synchronization issues
- If prototype successful:
 - LBNL mini-mosaic
 - Orthogonal Transfer CCD evaluation camera

CCD Prototype Status



2 fully assembled systems

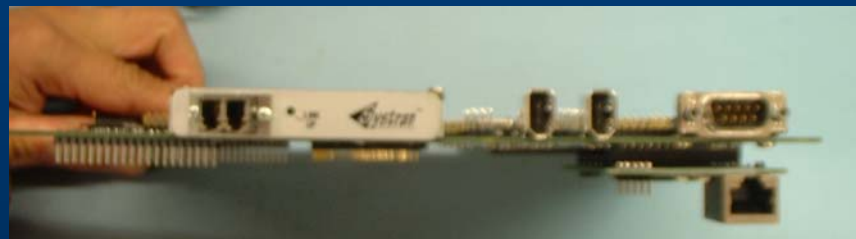
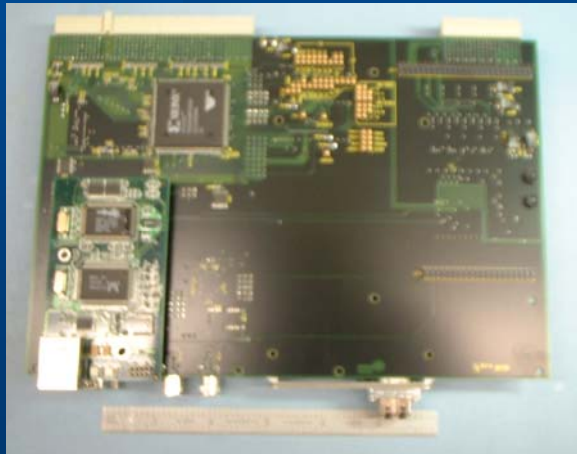
- Fiber network tested
- Clock & biases tested
- Acquisition channels under eval
- Component cost < \$5K
- Total power < 17 W



Master Control Board



- 3 PCBs fab'd, 2 PCBs assembled
- FPGA development in process
- Testing underway
- Component cost < \$ 5K
- Power < 12.5 W



IR 36 Channel Acquisition Board

- Design complete
- Layout complete
- Currently in PCB fabrication
- Currently in FPGA design phase
- Qty 2 prototypes in board assembly 5/25/02 – 6/7/02
- In board test 6/01/02 through 8/01/02

IR Clock & Bias Board

- Design in process
- PCB layout starting 6/24/02 thru 7/08/02
- FPGA design phase 5/25/02 – 7/01/02
- Qty 2 prototypes in board assembly 7/15/02 – 8/01/02
- In board test 8/01/02 through 9/01/02

MONSOON

Project Management

Barry Michael Starr

MONSOON within NOAO ETS Project Life Cycle

- 1) Concept Definition Phase
- 2) Proposal Phase
- 3) Conceptual Design Phase
- 4) Preliminary Design Phase (Here Now)
- 5) Critical Design Phase
- 6) Implementation Phase
- 7) Delivery/Installation Phase
- 8) Evaluation Phase
- 9) On Going Support Phase

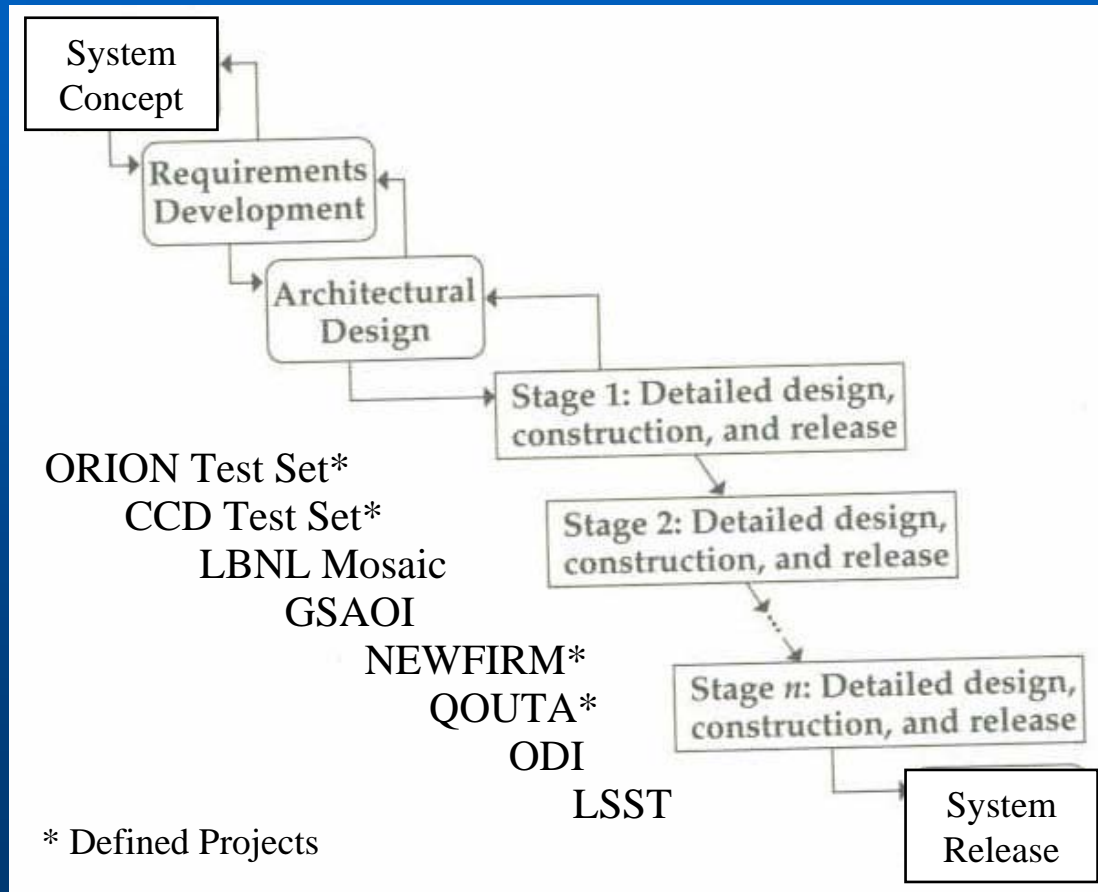
FOR MORE INFO...

ETS Standard Practice “Project Account Code System”

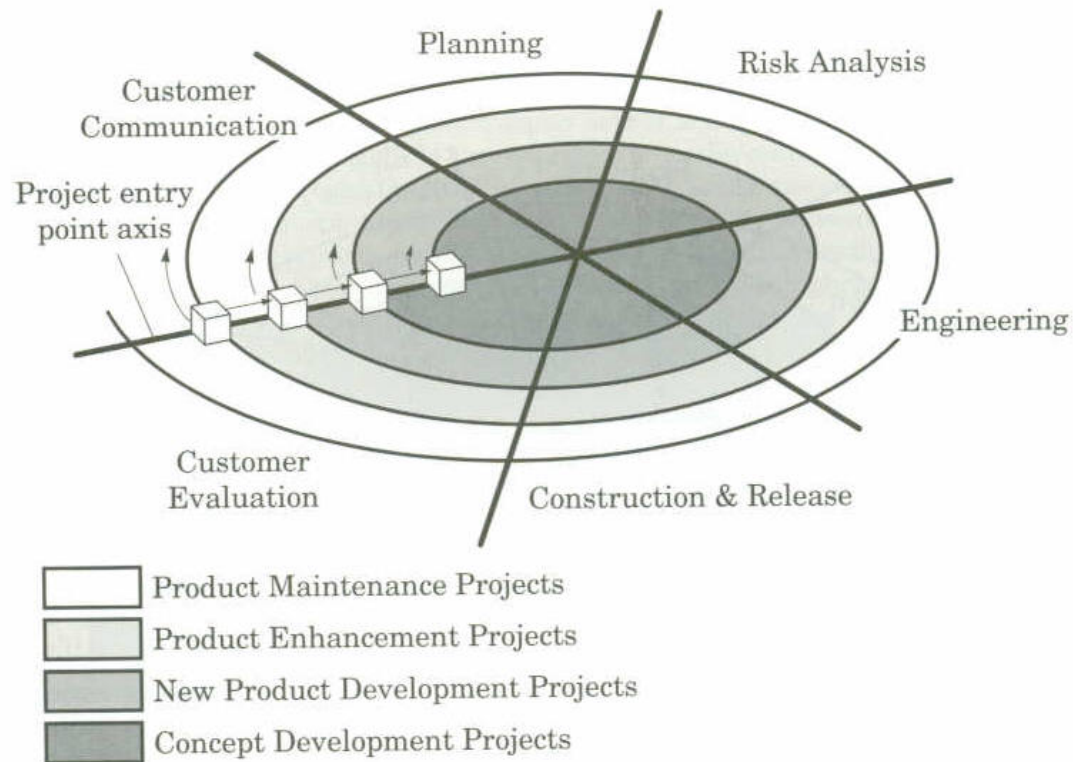
Component Based Development

- The MONSOON System Design has partitioned the system into HW & SW components
- Components are designed to be reused
- Components have well defined interfaces and functional requirements
- They are fully specified, built and tested standalone modules

Full MONSOON Project Will Be Phased Development



Spiral Software Development Lifecycle Model



MONSOON Project Staff FY '02

- Barry Starr – Project Manager / System Engineer (0.5 FTE)
 - Mike Merrill – Project Scientist IR (0.1 FTE)
 - Chuck Claver – Project Scientist OUV (0.1 FTE)
 - Nick Buchholz – Lead Software Engineer (0.75 FTE)
 - Gustavo Rahmer – Electrical Engineer (0.5 FTE) *
 - Jerry Penegor – Electrical Engineer (0.5 FTE) *
 - Dee Stover – PCB Layout, Doc Control (0.5 FTE)
 - Sang Nguyen – Electronics Technician, PCB Assy (0.5 FTE)
 - Yu-Min Ho – Engineering Intern (0.5 FTE) **
 - Kaviraj Chopra – Engineering Intern (0.25 FTE) **
 - Deepa Shroff – Software Engineer Intern (0.25 FTE) **
 - Henry Pang – Engineering Intern (0.5 FTE)
 - *Open position – Detector Engineer (0.25 FTE) ***
 - *Paul Schmitt – Electronic Technician (0.25 FTE) ****
 - *Ken Don – Electronic Technician (0.25 FTE) ****
 - *Phil Daly – Software (0.25 FTE) ****
 - CTIO Expert Consultants
 - Ricardo Schmidt @
 - Michael Warner @
 - Eduardo Mondaca @
 - Francisco Delgado @
- @: 0.1 FTE
- Outside Collaborators
 - ASTEROID
 - Steward
- * 0.75 FTE Jan – Oct
** 1.0 FTE May – Aug
*** 0.75 FTE July - Oct

MONSOON

Estimated Capital Expenditures '02

- 3 development platforms already in house
 - Dell PowerEdge PCs with GHz CPU & 512 MByte RAM
 - Systran SL100 links (PCI to CMC)
- 2 CCD Prototype boards fully assembled (4 PCBs total)
- 2 Master Control Boards fully assembled (3 PCBs total)
- 75% IR Prototype components purchased and received
- Estimated outstanding capital expenditures (\$ 50K)
 - Components (\$ 25K)
 - PCB Assemblies (\$ 10K)
 - Equipment/Software (\$ 15K)

MONSOON Board Costs

- Master Control Board
 - Board + components Cost: \$5K
 - Labor Cost (assembly & test): \$2K
 - Total Cost: \$7K
- IR Clock and Bias Board
 - Board + components Cost: \$2K
 - Labor Cost: \$3K
 - Total Cost: \$5K
- IR 36 Channel Acquisition Board
 - Board + components Cost: \$4.5K
 - Labor Cost: \$5.5K
 - Total Cost: \$10K

MONSOON System Costs

- ORION 64 Channel System
 - \$ 40K
- NEWFIRM 256 Channel System
 - \$ 125K
- GSAOI 16 Channel System
 - \$ 30K
- GSAOI 144 Channel System
 - \$ 80K
- QUOTA 32 Channel System *
 - \$ 25K
- ODI 512 Channel System *
 - \$ 300K

Note: Cost does not include NRE or System Specific Software

* Likely to require re-packaging due to WIYN mechanical requirements

SDSU for GSAOI Cost Estimates

- Scenario 1: (16 Ch System, SDSU2)
 - \$ 52,000
- Scenario 2: (128 Ch System, SDSU2)
 - \$ 384,500
- Scenario 3: (16 Ch System, SDSU3) *
 - \$ 22,000
- Scenario 4: (128 Ch System, SDSU3) *
 - \$ 130,500

(estimates do not include PC cost)

* SDSU 3 currently under development

Risk Management

- 4 Step Method

1) Identify 2) Evaluate 3) Avoid 4) Mitigate



- Continuous risk management process throughout project lifecycle.

Top 10 Risks

- 1) Lack of staff, staff allocated to other projects
- 2) Lack of organizational commitment
- 3) Undefined, unlimited project scope, or scope creep
- 4) PC data processing capability
- 5) Fiber-optic networks existence and performance
- 6) Mixed-signal components existence and performance
- 7) Development tools expense
- 8) Staff training – design, fabrication, test
- 9) Component obsolescence
- 10) Board fabrication densities.

Note: Risk Items 2 – 9 have been addressed

Risks According to ACM

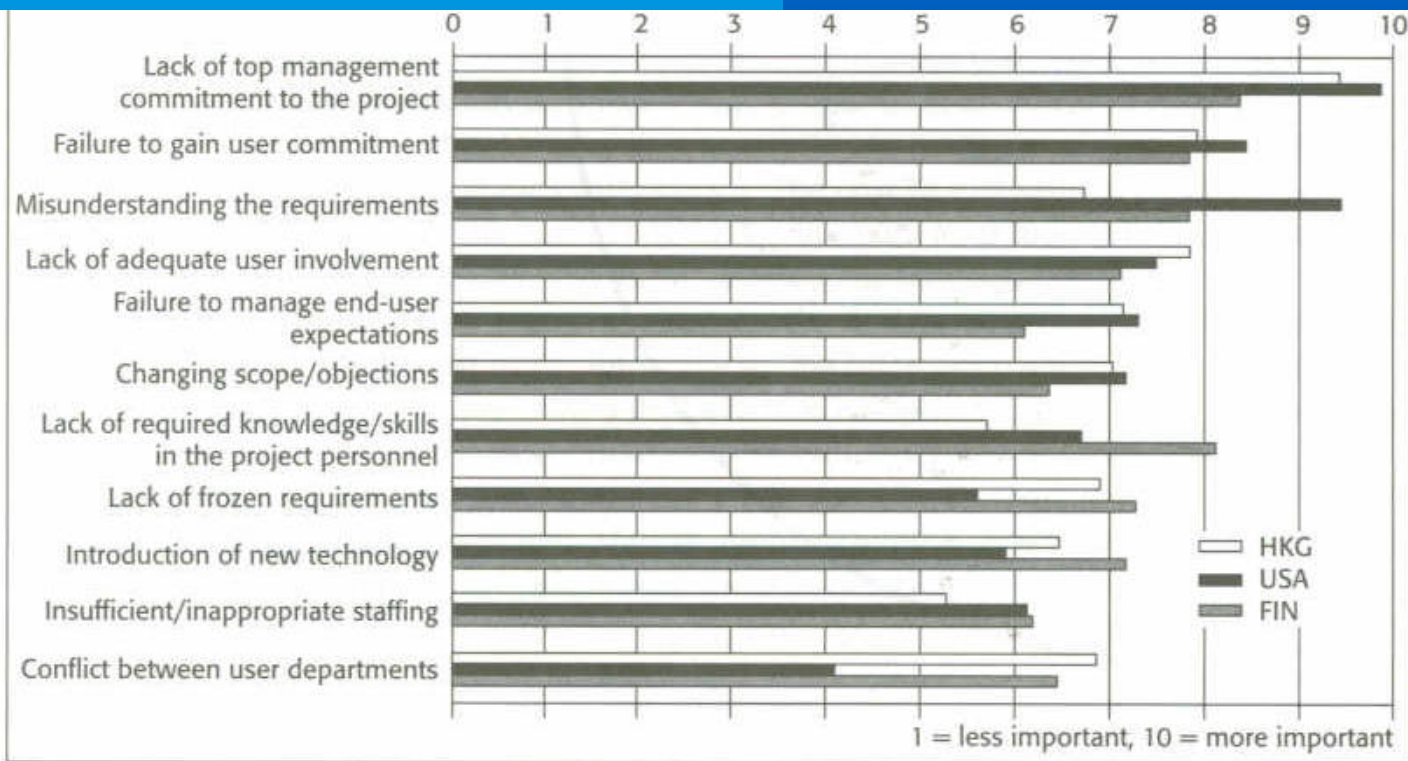


Figure 2.2 Risk factors identified by all three panels ordered by relative importance.

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Technology Risk Mitigation

- Modular system design (HW&SW)
 - Any risk element impact is limited to small area
- Component performance evaluation
 - Prototyping & benchmarks
 - Evaluate all key “risk” components through actual NOAO test
- Component obsolescence
 - Use “newer” technology from vendors with established user bases.
 - Modular design allows component upgrade or replacement
- Development tools
 - Use existing low-cost or no-cost design tools

All Technology Risk Issues Resolved

- PC data processing – Benchmarked August 2001
- Fiberoptic networks – Benchmarked March 2001
- 16-bit low power CMOS ADC technology – Tested July 2001
- FPGA development tools – In use since Nov 2001
- Surface mount fabrication technology – In use since 2001
- LabView Training – Oct 2001
- Prototype boards show needed densities (small form factor) – Nov 2001

Staffing Resource Risk

- Modular system design & well-defined interfaces.
 - Allows partitioning of work to multiple groups
- Use COTS to lower development efforts when appropriate.
- Plan the project for phased development.
- Use low-cost tools to allow wide participation by small groups.
- Acquire high-priority project standing within organization.
- Break sequential project component development cycle.
 - Software development not dependant on hardware
- Enlist collaboration with external groups => MONSTEROID

Test and Integration Plan

- Design & test to specification.
- Test procedure and test record for:
 - Each major component (HW&SW).
 - Each major subassembly.
 - Each complete end-to-end system configuration
- Distributed test of software components at multiple sites.
- Integrated test & config record maintained in web-based database
- Dynamic component & system test capability already developed at NOAO
- Tested over stated environmental conditions in FPRD
- Boards are individually assembled and tested, then integrated into DHE chassis where final system test is performed.
- System design supports easy integration and configuration

Quality Management

- Design to specification.
- Formal project review process (CoDR, PDR, CDR).
- Component level peer review (hardware & software).
- On-line test & configuration database.
- Extensive component & system test with burn-in time.
- Extensive system design and maintenance documentation
- Modular system design allows upgrades & component swapping when failures occur.
- Extensive system diagnostics provide for detailed failure determination and system health monitoring.

ORION Project Timelines

- MONSOON system specified & ordered Jan 2001
- MONSOON acquisition system delivery Aug 2002
- MONSOON full system delivery Nov 2002

- * ORION will use MONSOON Prototype IR System
 - 64 Channel, 16-bit 1MHz Acquisition

IR Project Timelines

- NEWFIRM

- MONSOON system specified & ordered Sept 2003
- MONSOON system delivery March 2004

- GSAOI

- MONSOON system specified & ordered Jan 2003
- MONSOON system delivery Jan 2004

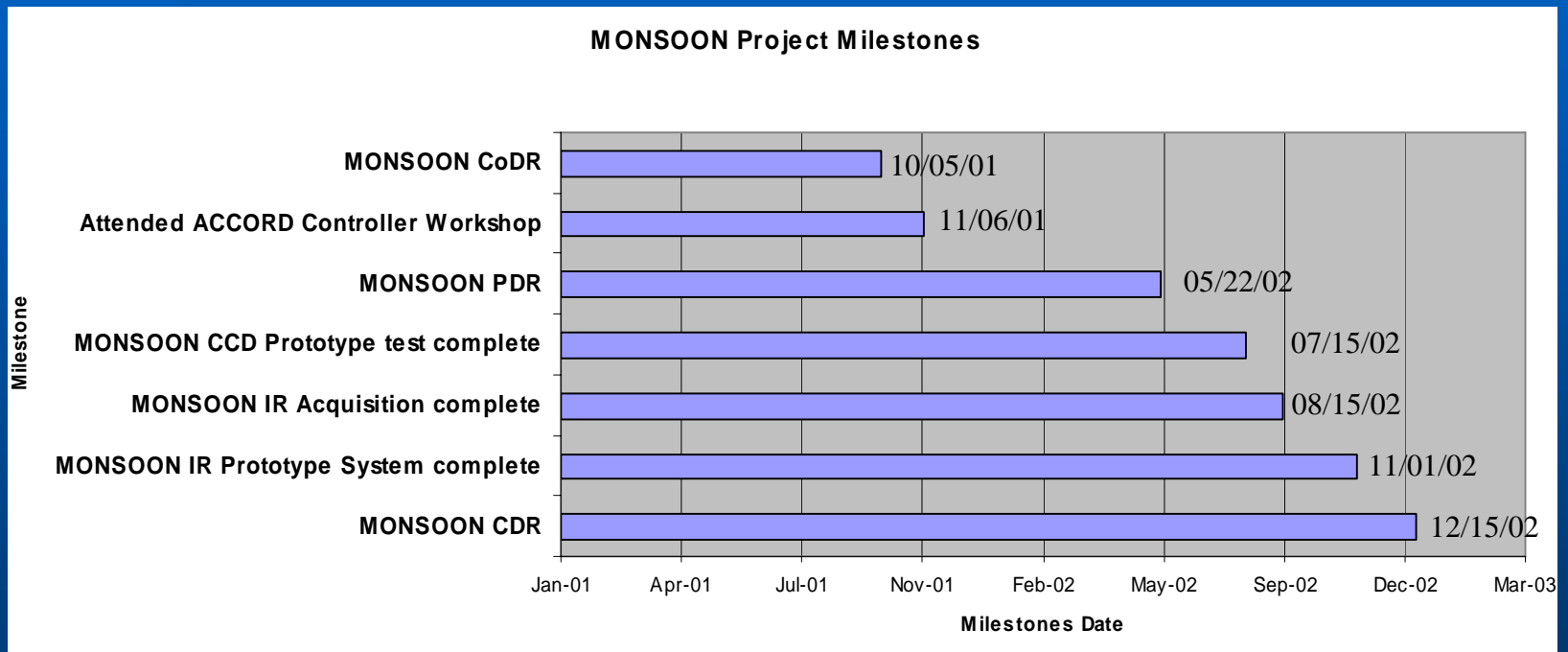
OUV Project Timelines

- QUOTA
 - MONSOON system specified & ordered TBD
 - MONSOON system delivery TBD
- ODI
 - MONSOON system specified & ordered TBD
 - MONSOON system delivery TBD
- LSST
 - MONSOON system specified & ordered TBD
 - MONSOON system delivery TBD

MONSOON Project Plan Milestones

- MONSOON CoDR 10/05/01
- Attended ACCORD Controller Workshop 11/6/01
 - at UCSC (LICK) to promote collaborative effort
- MONSOON PDR in 5/22/02
- MONSOON CCD Prototype test complete by 8/02
- MONSOON IR Acquisition complete in 8/02
- MONSOON IR Prototype System complete in 10/02
- MONSOON CDR in 12/20/02

MONSOON Project Plan Milestones



Note: Milestones Predicated on Full MONSOON Staffing

Project Plan

ID	Task Name	Dur	2000				2001				2002				2003					
			Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4			
1	Prototype Eval, Test Systems	80.8 w																		
2	Fiber optic Board Eval	12 w																		
3	PC Processing Eval	4 w																		
4	Dynamic Test System - Time Domain Test Capability	74 w																		
7	Dynamic Test System - Freq Domain Tests	10 w																		
10	Dynamic Test System - Histogram Tests	63 w																		
13	16-Bit ADC Eval	22.8 w																		
18	CCD Prototype Board	30.2 w																		
25	Master Control Board Prototype	29 w																		
32	32 Ch IR Acq Board Prototype (MotherBoard)	27 w																		
44	CCD Prototype Test Board	2 w																		
50	32 Ch IR Acq Proto Test Board	3.8 w																		
56	Arcview Eval	8 w																		
57	IR Clock & Bias Board Proto	18 w																		
64	IR Prototype System Integration (MCB-ACQ)	8 w																		
69	IR Prototype System Integration (MCB-ACQ-CLK)	5 w																		
74	CCD Prototype System Integration	6 w																		
79	DHE SW Simulator	4.4 w																		
85	Project Management	109 w																		
96	System Engineering	108 w																		
105	System Hardware	72 w																		
113	Detector Head Electronics	15 w																		
214	Software Design	38 w																		
225	Software Components	44.4 w																		
286	System Intgr. Test & Delivery	94.4 w																		
287	IR System Integration	6 w																		
292	Orion Test System Delivery	4.4 w																		
300	GSAOI System Delivery	52 w																		
308	NEWFIRM System Delivery	26 w																		

Maslow's Model Applied to Projects

