



4-bit EMBEDDED MPU based SEQUENCER

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Design Goals

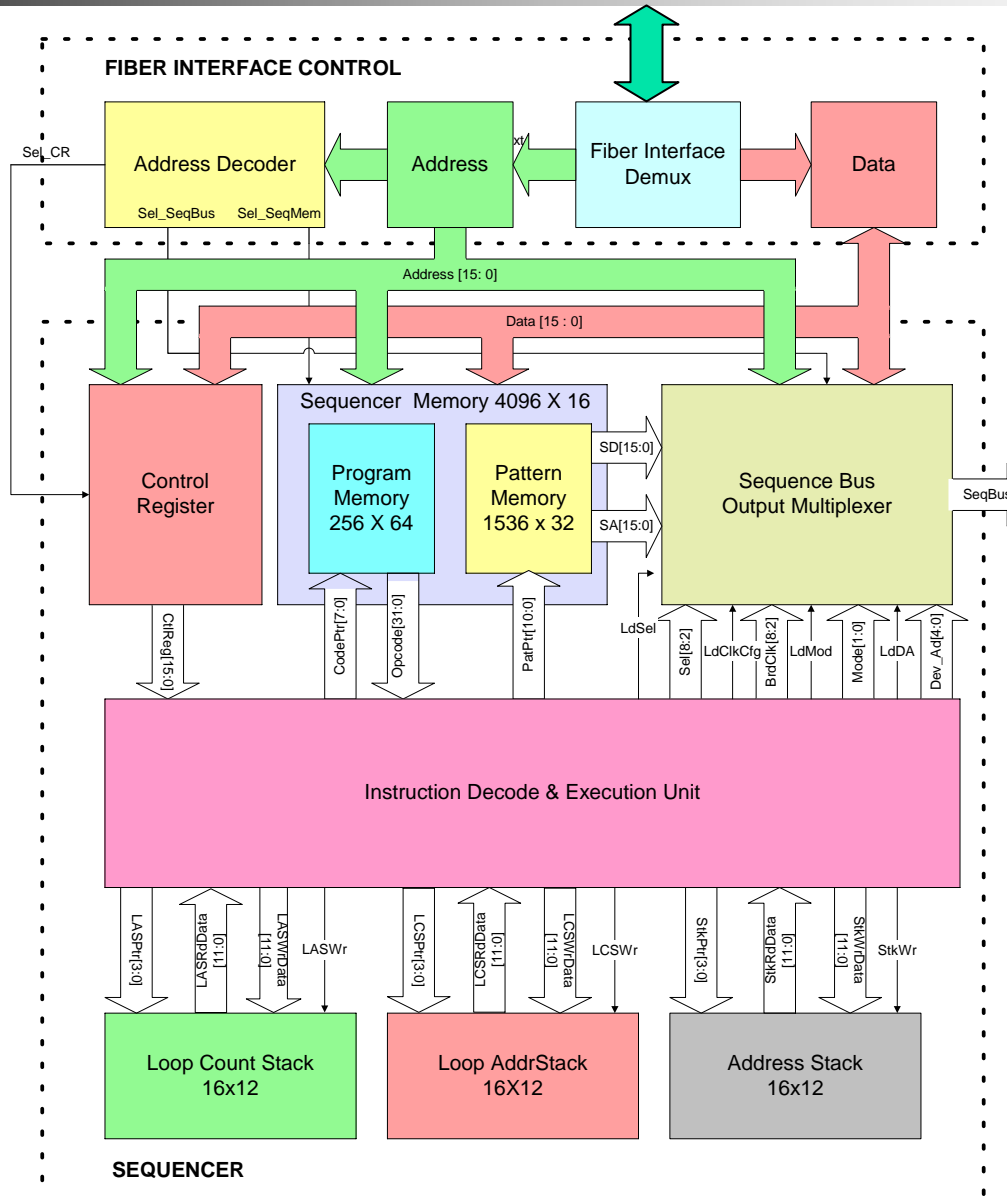
- Run time, Reconfigurability.
- A Generic MCB
- Support both Distributed and Centralised Control.
- Meet design time requirements.
Sequencer design is the `Critical Path`.



Possible Implementations:

- Finite State Machine based approach.
 - Optimal design with regards to logic density and timing requirements.
 - However fundamental design is locked. Limited reconfigurability of parameters possible. But to reconfigure control firmware has to be modified.
- Embedded MPU based approach.
 - Abstracts control from the firmware designer and provides complete system control to the designer at a higher level(PAN).
 - Reconfigurability in terms of both parameters and control is feasible at software level rather than firmware level.
 - The design approach is generic and is reusable for sub-ordinate boards like Clock and Bias Board with very few modifications.
 - Speeds up the so-called "CRITICAL PATH"(Design Plan Roadmap) and reduces the design time considerably.

Sequencer Architecture





4- BIT EMBEDDED MPU

- Control Requirements
 - Load Output Registers (Set)
 - Iteration (for & while)
 - Branching (if-else)
 - Delay (wait)



A. Load Output Instructions: (7)

1. LPP: Load Pattern Pointer: 4 Nibble (16 bit)
2. IPP: Increment Pattern Pointer: 1 Nibble (4-bit)
3. DPP: Decrement Pattern Pointer: 1 Nibble (4-bit)
4. LDA: Load Device Address (12-bit)
5. LMR: Load Mode Register 3 Nibble (12-bit)
6. LSR: Load Select Register 3 Nibble (12-bit)
7. LCR: Load Clock Register 3 Nibble (12-bit)



B. Branch and Loop Instructions: (5)

8. CAL: Call Subroutine : 4 Nibble (16 bit)
9. RET: Return 1 Nibble (4-bit)
10. JCB: Jump if Control Bit Set 5 Nibble (20-bit)
11. LPB: Loop Begin 4 Nibble (16-bit)
12. LPE: Loop End 1 Nibble (4-bit)



C. DELAY INSTRUCTIONS (4)

13. DUS: Delay micro Seconds 3 Nibble (12-bit)
14. DUS: Delay micro Seconds 3 Nibble (12-bit)
15. DSC: Delay System Clock 3 Nibble (12-bit)
16. NOP: No Operation 1 Nibble (4-bit)